SystemC UVM Verification Components

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Abstract

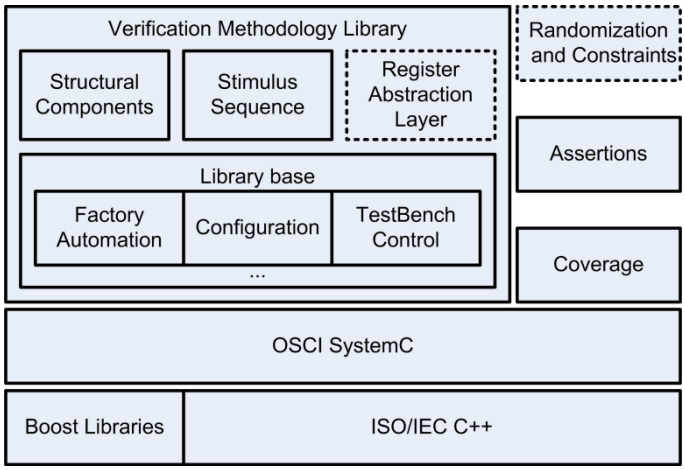
Though SystemC is widely accepted for development at higher abstraction levels, e.g. virtual prototypes, its verification capabilities are rather limited in comparison to other languages such as SystemVerilog. Therefore, we present an enhanced UVM for SystemC library which is originally based on the multiple-languages release of OVM (OVM-ML) which was donated by Cadence Inc. to ovm-world.org. Our verification library incorporates verification best practices from OVM-ML and UVM as well as project partner implementations. Moreover, we extended functionality and implemented missing features, such as SystemC simulation phasing alignment, domain specific components, stimuli sequence generation and management, call-back facilities, response to request routing, transaction recording, command-line processing for dynamic test bench loading and many more. Apart from that, we aligned our UVM for SystemC library with crucial verification components, such as functional coverage.

SystemC UVM Verification components – towards an *enhanced* UVM for SystemC

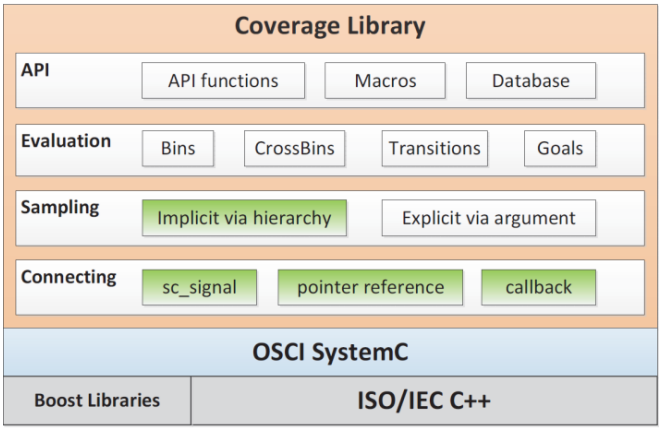
The base package contains structural verification components, which help to develop test and testbench environments in a disciplinarily way and expected structure. It includes **`Agents`**, **`Drivers`**, **`Monitors`**, **`Tests`**, **`Environments`**, **`Scoreboards`**, and **`Subscribers`**.

The library is designed for seamless integration into different verification flows and reuse of legacy verification components. It is EDA vendor independent as it was implemented to run with the standard IEEE-1666 SystemC simulator. Moreover, we pre-defined packages, intended to implement dedicated TLM verification features from our research partners such as:

- Assertions, Randomization/Constraint Solvers
- Functional Coverage



SystemC UVM and verification components



Structure of the functional coverage library package

As first package we integrated a functional coverage library, which implements large portions of the functional coverage functionalities of the IEEE-1800 SystemVerilog standard. Hence, we improve the SystemC verification features and enable the coverage-driven verification (CDV) paradigm to determine verification closure. We believe that enabling CDV in SystemC design flows in conjunction with the usage of efficient UVM testbench structures will boost SystemC's role as high-level design and verification language (HLDV), in doing so, still being a fully free of charge and open source ecosystem.

Acknowledgement

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