Evolvable Hardware FPGA-based platform for Autonomous Fault-tolerant Systems

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Evolvable Hardware (EH) is a technique that consists on the use of reconfigurable hardware devices whose configuration is controlled by an Evolutionary Algorithm (EA). In this demonstration we show an EH platform where the full system is implemented in the FPGA. Figure 1 shows the architecture of the proposed System-on-Chip (SoC), consisting on a MicroBlaze processor responsible of controlling the whole system operation, a Reconfigurable processing Core (RC) and a Reconfiguration Engine (RE).

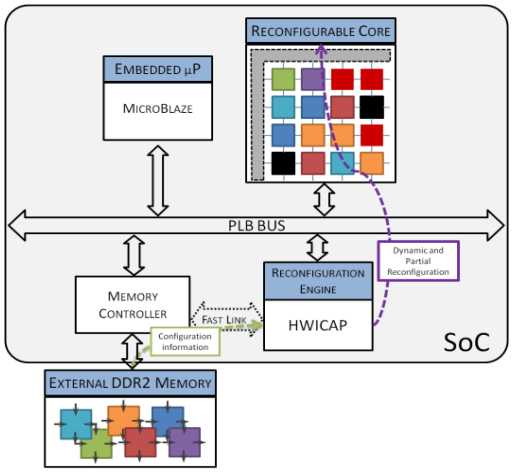

Figure 1. Overview of the System Architecture

The RC architecture is based on a two dimensional mesh-type systolic array of parallel Processing Elements (PEs). Each PE is a basic computational unit able to perform a single operation on the data taken from their close neighbors, in one clock cycle. Each PE includes a Functional Block that performs a basic operation with the input signals, and sends the result through its both outputs. A major feature of our proposal is the possibility to change the functionality of the PEs by means of DPR, among those included in an external library.

A RE for the low level control of the Internal Configuration Access Port (ICAP) has been also included. The main advantage of this reconfiguration engine is the relocation capability implemented in hardware, which also includes the readback/reallocation/writeback approach. It has been designed to be times faster than the evaluation phase of the candidate circuit, even beyond the maximum theoretical throughput of the reconfiguration port. Further details regarding the system architecture can be found in [1].

A *(1+λ) Evolution Strategy* with 1 parent and λ offspring has been implemented as the EA running on the MicroBlaze.

Proposed Demonstrator setup includes the FPGA, where the system described above is implemented, an external laptop, in charge of the initial configuration of the FPGA and an independent screen, as appears in Figure 2. As shown in captures provided in Figure 3, in the screen, filtered images obtained from the Reconfigurable Core during the evolution process are printed at run-time. It allows proving the suitability of EH techniques to autonomously design image filters. In addition, the progression of the fitness, measuring the quality of the designed circuit, is depicted. The Processing Elements configured within each position of the RC at each moment are also shown, until the final circuit is reached. Images used both as the golden reference and the noisy inputs, as well as their level of noise, can be selected in advance of launching the process. Some parameters of the EA can be changed as well. Demonstrator also includes advanced features of the EH platform, like the improvement of the filtering results when several filters are cascaded (Obtained after a single evolution process).

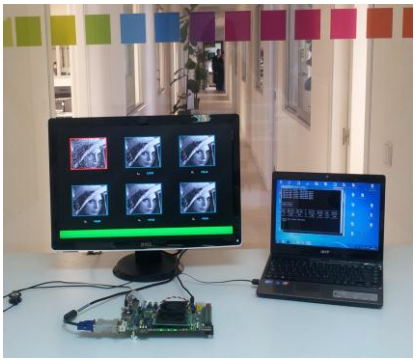

Figure 2 Demonstration Setup

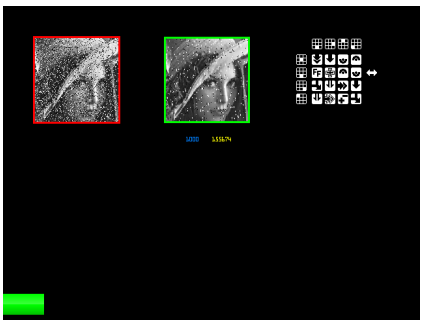

Figure 3 Screen Captures during the Evolution Process

Furthermore, the Fault tolerance and recovery feature of the designed autonomous platform described in [2] is also shown. This behavior enables self-healing capabilities against both transient and permanent faults. A quite good response to cumulative faults is also demonstrated. In the demonstrator, the damage of a Processing Elements of the array can be selected, while the recovery process of the array can be observed at run-time. Depending on the specific EA parameters, each demonstration running takes between 2 or 3 minutes.

REFERENCES

[1] Otero, A.; Salvador, R.; Mora, J.; de la Torre, E.; Riesgo, T.; Sekanina, L.; , "A fast Reconfigurable 2D HW core architecture on FPGAs for evolvable Self-Adaptive Systems," NASA/ESA Conference on Adaptive Hardware and Systems (AHS), 2011

[2] Salvador, Ruben; Otero, Andres; Mora, Javier; Torre, Eduardo de la; Sekanina, Lukas; Riesgo, Teresa; , "Fault Tolerance Analysis and Self-Healing Strategy of Autonomous, Evolvable Hardware Systems," International Conference on Reconfigurable Computing and FPGAs (ReConFig), 2011