Multiplierless Design of Low-Complexity and High-Speed DSP Systems

The multiplication of data samples with constant coefficients is a ubiquitous operation and performance bottleneck in many Digital Signal Processing (DSP) systems, such as digital Finite Impulse Response (FIR) filters, Discrete Cosine Transforms (DCTs), and filter banks. Since the realization of a multiplication operation in hardware is expensive in terms of area, delay, and power dissipation and the constants to be multiplied by variable(s) are determined by the DSP algorithms beforehand, the constant multiplications are generally implemented in a shift-adds architecture where each constant multiplication is synthesized using addition, subtraction, and shift operations. Hence, the fundamental optimization problem is defined as finding the minimum number of addition and subtraction operations that realize the constant multiplications.

Although the minimization of the number of operations reduces the complexity of a design, it is not guaranteed that it always yields a design with optimal area at gate-level. Hence, high-level algorithms should take into account the gate-level implementation cost of each addition and subtraction operation. The algorithms should also be capable of considering different design platforms (ASIC or FPGA), design architectures (digit-serial or bit-parallel), and adder types (ripple carry adder or carry-save adders).

Performance is also a crucial parameter in many DSP systems and circuit area is generally expandable in order to achieve a given performance target. Although the delay parameter is dependent on design architectures and implementation issues, the delay of a shift-adds design of constant multiplications is generally considered in terms of the number of adder-steps, which denotes the maximal number of adders and subtracters in series. Hence, in order to find the optimal tradeoff between area and delay, the high-level algorithms should be capable of finding a solution under a delay constraint. This feature also enables us to find low-complexity and high-throughput pipelined designs.

Power consumption has become a matter of concern with the increasing popularity of portable electronic devices, including many DSP systems. In the multiplierless design of constant multiplications, power dissipation is highly related to the depth and gate-level area of each addition and subtraction operation. Hence, in order to reduce the power dissipation, the high-level algorithms should consider these metrics in the synthesis of constant multiplications.

This work is supported by the *Portuguese Foundation for Science and Technology* (FCT) research project *Multicon - Architectural Optimization of DSP Systems with Multiple Constants Multiplications*. The details on the *Multicon* project can be found at http://algos.inesc-id.pt/multicon.