The COMPLEX Eclipse Framework for UML/MARTE Specification of Embedded Systems and Automatic Generation of Executable Models for Design Space Exploration

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The high complexity and variety of applications and platforms in current embedded systems is tackled by ESL design methodologies by means of several advanced concepts and languages. In the first and critical system specification step, the adoption of the Model Driven Engineering (MDE) principles make possible to raise the abstraction level in the development process and take advantage of automation capabilities to generate implementation code and analysis models. Moreover, the UML language and the recent MARTE profile enable a standardized way for describing the system. The standard SystemC language, Transaction Level Modeling (TLM), and modern performance analysis techniques, such as native simulation or virtualization, have enabled the building of fast executable models for functional validation and performance analysis. Fast performance analysis models are crucial for tackling the design space exploration (DSE) activity, in order to do early right decisions from a wide design space.

This demo booth will present the COMPLEX Eclipse-based UML/MARTE ESL design framework, developed by the Microelectronics Engineering Group of the University of Cantabria (GIM/UC) (www.teisa.unican.es/gim) jointly with GMV (www.gmv.com) in the COMPLEX (COdesign and power Management in PLatform-based design space EXploration) FP7 project. This framework integrates the aforementioned design principles, and provides innovative enhancements, such as separation of concerns and the description of the design space embedded in the architectural description of the system.

Specifically, the demo booth will focus on the UML/MARTE modelling, using an Enhanced Full Rate (EFR) vocoder fully compliant with the GSM standard as example, and on the automated generation of the executable performance model for functional validation and for fast performance analysis.

First, the demo will show how the whole EFR Vocoder is specified, including its functionality, split into components, and how the architecture of the application is described. The demo will also highlight how the SW/HW platform is described, and the architectural mapping (i.e. allocation of the application components to the platform resources). Special remark will be put on the presentation of the capability of the specification methodology for the definition of the design exploration space. That is, the model built actually represents several implementation solutions, defined through the use of design parameters (e.g., frequencies, number of cores, etc), rules and constraints that define a set of architectural solutions that define the design exploration space. It will be also shown how to specify the output metrics to be analysed, such as power consumption and application latencies.

In a second part, the demo will demonstrate how the executable performance model is simply and automatically generated through the Eclipse-based environment. Additionally, it will highlight the insights on how this automation level is achieved through a set of model-to-text generators, and the mechanisms that permit the framework to be customized with new analysis and transformation engines. The attendee will also see the generated executable model, its fast simulation, and how the simulation enables a bit accurate functional validation. Moreover, the performance output data, and the output formats, which make this framework especially suited for DSE, will be shown.