Optimizing and validating high level design parameters of ADC for PA Linearization

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I. Introduction

Power amplification of signals with non constant envelope usually creates distortions in the signal due to the nonlinear characteristics of power amplifiers (PAs). To meet the wireless communication standards requirements, correction techniques should be employed. The digital predistortion (DPD) offers an efficient solution to linearize PAs. Its main part is implemented in digital domain which makes it more and more popular.

This technique requires the insertion of a feedback path to collect the distorted signal and a digital processing part before the RF power amplifier to perform the calculation of the inverse response of the PA then apply the correction (Fig. 1).

The analog-to-digital converter (ADC) of the feedback path is a key element of the DPD. It should achieve the required resolution for the correction algorithm while maintaining lowest possible complexity and power consumption.

Unlike in classical systems, the constraints on this type of ADC are harder to define due to the highly non linear processing of the DPD algorithms and to the lack of CAD tools adapted to this application.

In this demonstration we use a commercial tool to perform system simulation of a DPD system thereby allowing us to optimize the ADC parameters.

II. Demonstration Setup

We will demonstrate these system simulations on a computer running the Agilent's SystemVue software. The software provides behavioral models and complete Physical Layer (PHY) libraries for the advanced communication standards such as 3GPP WCDMA, the standard that will be used for the demonstration.

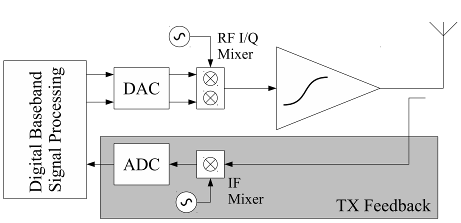

Fig. 1. Digital Predistortion Block Diagram

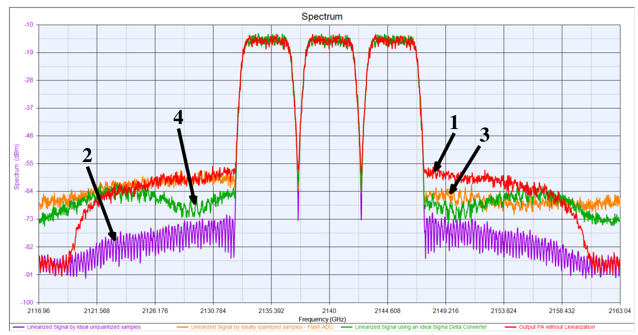

Fig. 2. Simulated output spectrum for systems without DPD and with ideal and quantized data DPD : 1- Distorted Ouput PA ; 2- Linearized Signal by ideal unquantized samples ; 3- Linearized Signal using flash ADC ; 4- Linearized Signal using ΣΔ converter

III. Demonstration Experience

In this demonstration, we show the impact of the ADC resolution on the performance of the DPD. We use as a test case a multi-carrier WCDMA scenario. Two types of ADCs are investigated : flash and ΣΔ.

We will explain the different steps of the DPD system in the simulation environment. After, we will show the effect of quantization on the DPD with a flash ADC in the feedback path (Fig. 2). This simulation environment allows us to find the minimmal resolution ADC to meet the Adjacent Channel Power Ratios (ACPR) standard requirements. Then, an equivalent ΣΔ converter will be used to check the feasibility of such a solution.

IV. Conclusion

We used the Agilent's SystemVue software to model a multi-carrier 3GPP WCDMA basestation transceiver. The software built-in DPD algorithm allows us to emulate the performance of the entire power amplifier DPD loop and to evaluate the specification of the feedback ADC.

Acknowledgment

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http://www.catrene.org/web/projects/project_list.php