TASERS
Time and Space Separated Embedded Real-time System with Shared SDRAM

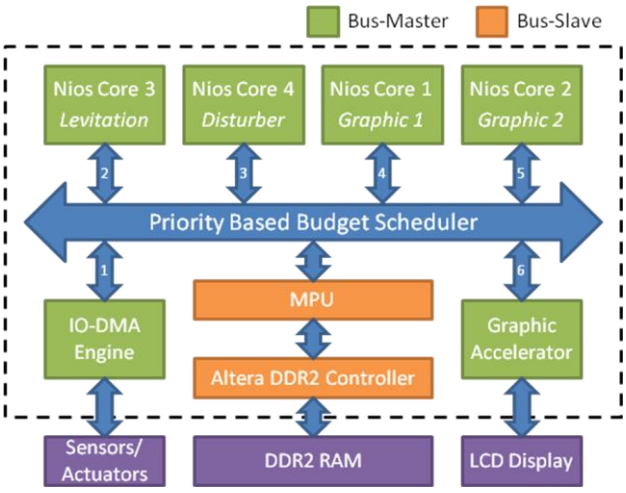
Our demonstrator exhibits time and space separation in a multi-core system with shared DDR2 memory. The technique can readily be used in safety critical or mixed critical systems where applications have equal or distinct memory bandwidth, latency and space requirements.

Temporal separation on the shared SDRAM is provided by Priority Based Budget Scheduler*. The arbiter offers low latency access to the shared SDRAM as well as satisfies distinct bandwidth requirements of various applications.

*[H. Shah, A. Raabe, A. Knoll. Bounding WCET of Applications Using SDRAM with Priority Based Budget Scheduling in MPSoCs. DATE'12.]

Spatial separation is provided by a shared memory protection unit. This unit is located between the shared memory and the system bus. The type of request (read/write), the requesting core and the target address are matched against a permission table.

The following applications run on the demonstrator:



- **Graphics** – Memory Intensive Firm Real-time:
  - Two separate processors control each rectangular boundary
  - tokens from both the boundaries must join accurately
  - The tokens move 1 pixel / frame
  - Both processors synchronize only once after the reset
  - synchronization is controlled only by memory bandwidth each core receives
  - A separate hardware accelerator dumps the frames from the SDRAM onto the LCD
- **Levitation** – Latency sensitive hard real-time:
  - A dedicated processor controls the levitator (deadline - 10 ms)
  - Samples from hall sensor are buffered in the SDRAM
- **Disturber** –Application simulating a "babbling idiot" trying to corrupt the other applications:
  - Causes glitches on the LCD display by writing into the graphic memory
  - Disturbs the flying bar by congesting the bus

In our demonstrator each of the separation mechanisms can be enabled separately. The effect can be seen by the behaviour of the applications:

- **Temporal separation:**
  Influence of the Disturber to the flying bar and the synchronisation of the tokens is prevented.
- **Spatial separation**:
  Disturber can no longer write to memory of the rotating rings. Glitches on the display disappear are prevented.

Hardware: Altera Cyclone III FPGA Development Board, NIOS II – e Processors, Single Threaded, @ 125 MHz, HSMC Multimedia Board from Terasic, HSMC GPIO ADC Card

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