MIMO Detection-Decoding Engine for 4G Wireless

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Motivation

In current and future wireless standards, such as WiMAX, 3GPP-LTE or LTEAdvanced, receiver terminals have to support numerous operating modes for each protocol, as well as sophisticated transmission techniques, especially enhanced MIMO detection and iterative forward error correction (FEC). MIMO detection and FEC belong to the most computationally complex parts of the receiver-side baseband signal processing chain. Implementations thereof must have low power consumption, but also be able to interact in a flexible and efficient way in the detection-decoding engine, while at the same time not compromising on the challenging throughput and flexibility requirements associated with 4G standards.

Designing flexible, high-throughput and cost-effective VLSI detectors represents a challenge in multi-antenna spatial multiplexing systems with high constellation orders (e.g. 4×4 MIMO, 64-QAM). Conventional low-complexity detectors using, for example Successive Interference Cancelation (SIC), provide poor BER-performance, whereas exhaustive-search algorithms (full max-log-APP detection) cannot meet 4G data rates nor reasonable hardware complexity. Major FEC challenge for 4G wireless is the requirement to support more than one coding type – typically a combination of convolutional, Turbo, Reed-Solomon, or LDPC codes. For this purpose, several independent IP cores are usually utilized, resulting in unnecessary overhead which possibly can be mitigated by combining the decoding capabilities for different code types into one decoder.

Demonstrator

In this demonstrator, we present an efficient, high-throughput detection-decoding engine for 4G communications. It is comprised of a FEC module supporting LDPC and Turbo decoding and a MIMO sphere detector (SD) module supporting up to 64-QAM and 4x4 MIMO systems. Both modules are implemented within the 'Tommy' MPSoC and connected via a packet-switched NoC, allowing SD and FEC to be used as stand-alone units or as an integrated detection-decoding chain. The provided data rates of up to 923 Mb/s by the SD and 335.4 Mb/s by the multi-mode FEC make them the first silicon implementations of their kind to fulfill the 4G throughput requirements.

The demonstrator consists of a board hosting the chip, connected to a host computer running a communications system modeled in Matlab (Fig. 1). The chip receives the data generated by the Matlab's communication chain, executes the detection and decoding on the SD and FEC modules and transfers the output data back to Matlab. The developed graphical user interface (GUI) allows selecting different configurations of the SD-FEC engine and evaluating the resulting bit error rate (BER) performance. Additionally, power consumption for different voltage and frequency configurations is measured and depicted. The core supply voltage is adjustable from 1.1V-1.35V for the entire chip, and the operating frequency is also configurable from 83MHz-500MHz. This configurability allows analyzing BER and energy scaling under different transmission and supply conditions.

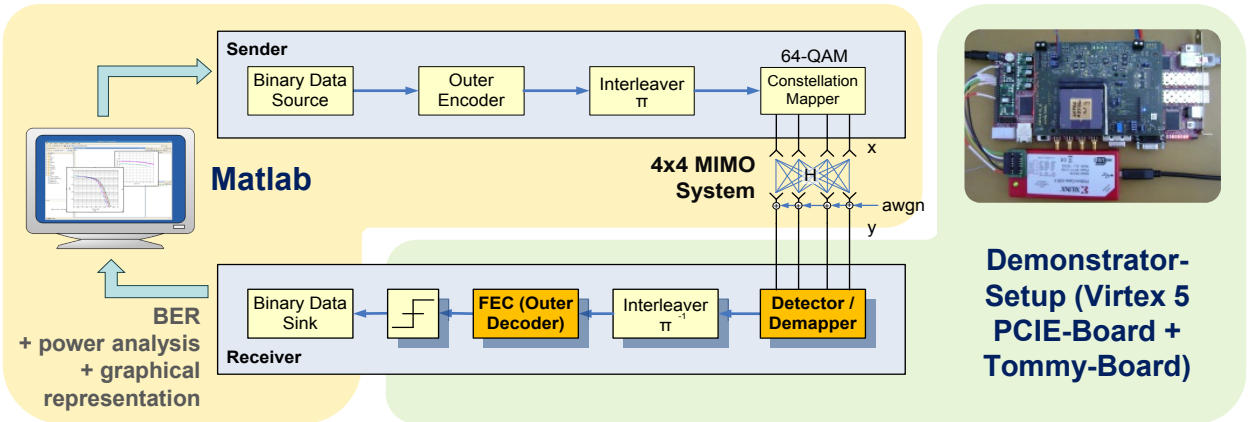

Fig. 1: Demonstrator communication system chain

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03/2012