

VisualHDL: Bringing C++ productivity to VHDL world

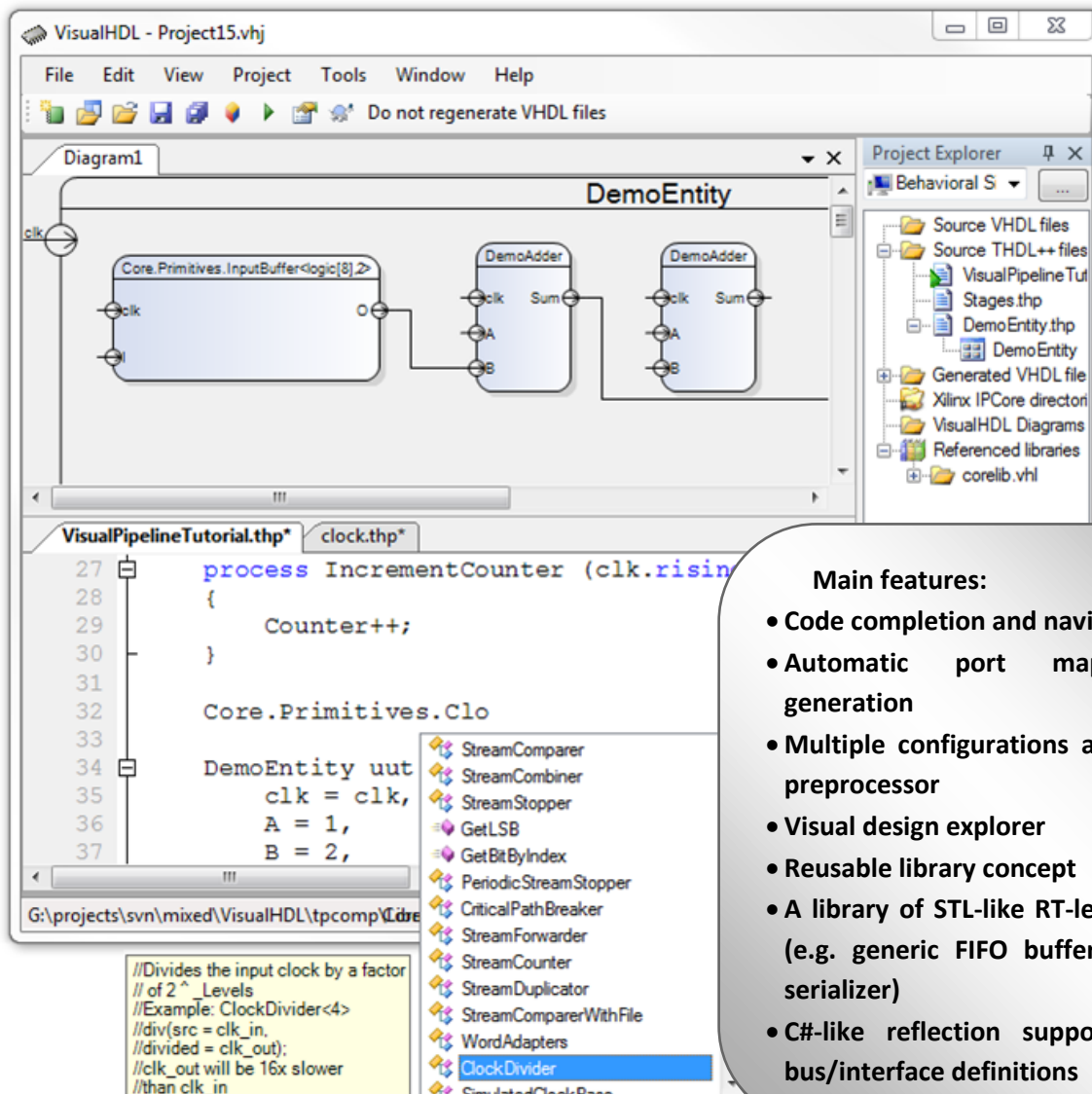
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C++: high-productivity, reusable, maintainable, tons of IDEs

VHDL: full control, massively parallel, industry standard



Idea: Combine the best from both worlds!



The screenshot shows the VisualHDL software interface. The top window displays a block diagram titled "DemoEntity" with components like "Core.Primitives.InputBuffer", "DemoAdder", and "DemoAdder". The bottom window shows VHDL code for "IncrementCounter" and "DemoEntity uut". A component library is visible on the right, listing various blocks like "StreamComparer", "StreamCombiner", and "ClockDivider".

```
27 process IncrementCounter (clk.rising)
28 {
29     Counter++;
30 }
31
32 Core.Primitives.Clo
33
34 DemoEntity uut
35     clk = clk,
36     A = 1,
37     B = 2,
```

Main features:

- Code completion and navigation
- Automatic port map template generation
- Multiple configurations and a C++-like preprocessor
- Visual design explorer
- Reusable library concept
- A library of STL-like RT-level templates (e.g. generic FIFO buffer with record serializer)
- C#-like reflection supporting generic bus/interface definitions

The tool is freely available online under <http://visualhdl.sysprogs.org/>