Design Space Exploration for Modern Automotive Ethernet-based E/E Architectures

Felix Reimann, Sebastian Graf, Michael Glaß, and Jürgen Teich
University of Erlangen-Nuremberg, Germany
{felix.reimann,sebastian.graf,glass,teich}@cs.fau.de

***Abstract*—Presented is a system-level design framework for complex automotive ECU networks, particularly considering upcoming communication technologies like *Ethernet AVB*. A sound tool flow is achieved by coupling a state-of-the-art ESL framework with an established CASE-tool from the automotive domain. The design space exploration is hereby equipped with novel symbolic synthesis techniques as well as simulative (virtual prototyping) and analytical (Modular Performance Analysis) timing analysis approaches.**

I. Introduction

Future automotive E/E architectures consist of more than 100 *Electronic Control Units* (ECUs), numerous sensors and actuators, as well as a complex communication architecture comprising a heterogeneous bus system that is connected via gateways. As the commitment to a specific configuration of the used hardware and software-architecture is a very challenging task which can hardly be performed by a developer. Thus, Computer-Aided Design tools (CAD) are required in the overall development process to handle the huge design space. Especially the optimization of the E/E architecture has to deal with several different networking standards like upcoming IP-based communications [2] and many new technologies like Ethernet and Ethernet AVB [5]. Thus, an automatic *design space exploration* tool to optimize such networks must be able to handle all the available bus technologies and, moreover, guide the developer to high-quality system implementations.

II. Concepts

The specification we use as input is modeled in PREEvision [1], a widely used CASE-tool for designing E/E architectures. PREEvision allows to independently model the functional as well as the component network. The problem for the design space exploration is given by additionally adding a degree of freedom for task binding and message routing. Moreover, to find the optimal implementation, we also search for the best priorities, AVB traffic classes, CAN and FlexRay parameters. To cope with the huge resulting design space, we use recent technologies from meta-heuristic research, see [6]. Thus, our design space exploration is able to find appealing solutions for real-world case studies.

The optimization objectives are monetary costs, power consumption, and timing properties which are measured with simulative and analytical approaches. The SystemC simulation is based on high level virtual prototypes, creating an executable system specification [8] to model the system behavior in conjunction with the selected system hardware [4]. The analytical evaluation, which can provide information about the best and worst case behavior of the system [7] is used to assure that the system works in the specified bounds. Additional evaluators that consider reliability [3] or dynamic energy consumption as well as third party tools can be seamlessly integrated according to the demands of the designer.

This work was supported in part by the German Federal Ministry of Education and Research (BMBF) under project 01BV0914-SEIS.

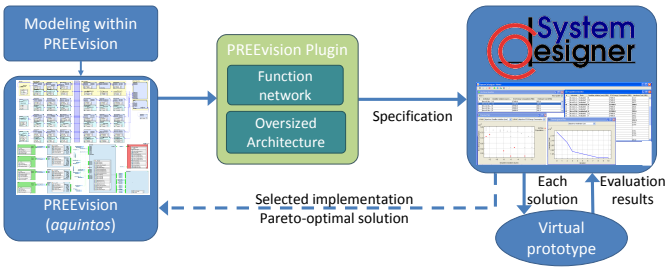

Fig. 1. Visualization of the established Toolflow. Starting from an existing model in PREEvision, the plugin extracts all required information for the design space exploration within the SystemCoDesigner. For the evaluation of each solution, a virtual prototype is used. Finally, the designer is able to select a pareto-optimal solution and reintegrate it in PREEvision.

References

[1] aquintos GmbH. Preevision. http://www.aquintos.com.
[2] M. Glaß, D. Herrscher, H. Meier, M. Piastowski, and P. Schoo. SEIS – Security in Embedded IP-based Systems. *ATZelektronik worldwide*, 1:36–40, 2010.
[3] M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt, and J. Teich. Symbolic Reliability Analysis and Optimization of ECU Networks. In *Proc. of DATE'08*, 2008.
[4] S. Graf, M. Streubühr, M. Glaß, and J. Teich. Analyzing Automotive Networks using Virtual Prototypes. In *Proc. of Automotive meets Electronics 2011*, pages 10–15, Dortmund, Germany, 2011.
[5] The Institute of Electrical and Electronics Engineers, Inc., 3 Park Avenue, New York, NY 10016-5997, USA. *IEEE Standard for Local and metropolitan area networks – Virtual Bridged Local Area Networks*, IEEE Std 802.1qav-2009 edition, Jan. 2009.
[6] M. Lukasiewycz, M. Glaß, F. Reimann, and J. Teich. Opt4J – a modular framework for meta-heuristic optimization. In *Proceedings of the Genetic and Evolutionary Computing Conference (GECCO 2011)*, Dublin, Ireland, July 2011.
[7] F. Reimann, A. Kern, C. Haubelt, T. Streichert, and J. Teich. Echtzeitanalyse Ethernet-basierter E/E-Architekturen im Automobil. In *GMM-Fachbericht – Automotive meets Electronics (AmE 2010)*, volume 64, pages 9–14, 2010.
[8] M. Streubühr, J. Gladigau, C. Haubelt, and J. Teich. Efficient Approximately-Timed Performance Modeling for Architectural Exploration of MPSoCs. In D. Borrione, editor, *Advances in Design Methods from Modeling Languages for Embedded Systems and SoC's*, volume 63 of *Lecture Notes in Electrical Engineering*, pages 59–72. Springer Netherlands, 2010.