GSNOC - A Generic Scalable Simulation Framework for 3-Dimension Networks-on-Chip

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***Abstract*—3D ICs are emerging as a promising solution for scalability, power and performance demands of next generation Systems-on-Chip (SoCs). Along with the advantages, it also imposes a number of challenges with respect to cost, technological reliability, thermal budget and so forth. Networks-on-chips (NoCs), which are thoroughly investigated in 2D SoCs design as scalable interconnects, is also well relevant to 3D IC Design. The cost of moving from 2D to 3D should be justified with improvements in performance, power or latency. We developed a framework that can support 2D and 3D NoCs system simulation and evaluation. Users can select different design parameters (i.e. buffer size, topology (different number of TSVs for 3D), architecture, routing algorithm, area size and technology). We established a generic scalable pseudo application (GSPA) and included a wide range of state-of-the-art benchmarks to provide the sufficient complex scenarios for NoCs exploration. These test scenarios can also be used for mapping, placement and scheduling research as application models. A Graphic User Interface (GUI) has been built for the framework. Users can observe the system and local behavior while the simulation processing, e.g. the state of the Processing Elements (PE) and buffer (distributed memory) demands for the application traffic scenarios and given constrains. We also created a real 3D communication monitor, which can support users to obtain a straight view of the utilization of each link in the overall 2D and 3D systems. After the simulation, the detailed evaluation report will be generated automatically, which include all the NoCs system configuration information, the overall time demand of the simulation, throughput, distributed memory demands, links utilization, system interconnect power and energy consumption, TSV utilization and so forth. We employed this framework to build a FPGA prototype demonstration, and have shown that the real-time hardware emulation results and the framework simulation results are consistent.**

***Keywords*-3D NoC; Framework; Simulation; Evaluation; Vertical Channel Density (VD); Graphic User Interface (GUI);**

I. Framework Overview

This paper presents a simulation framework for 3D NoCs where users have full flexibility from generating their own generic pseudo scalable applications to selecting vertical channels (TSVs) densities (VD) according to their technological constraints. The framework will provide throughput, latency and power numbers evaluation for the specific configuration. Designers will get a range of design points to select which can fulfill their design specifications.

Figure 1 shows the logic structure of the framework. Users can select the technology depending on their area and power requirements. A Generic Scalable Pseudo Application (GSPA) as well as a collection of state-of-the-art benchmarks are available to simulate and evaluate the NoC system. Different NoC routers and IPs can be selected by the users based on the component library. From the topology point of view, users are allowed to specify their own 2D and 3D design. Especially in 3D topology, users can specify different vertical

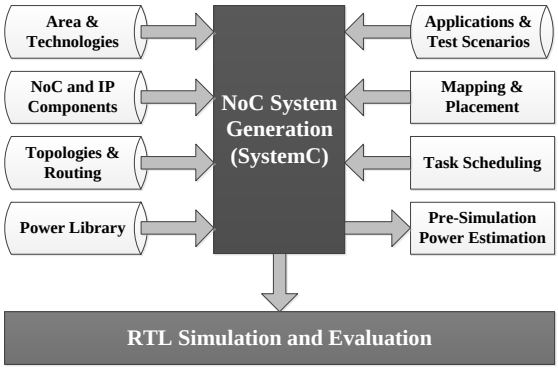

Fig. 1. Simulation Framework Flow

channel densities according to their demands. The framework is developed in a modular way so that users can easily plug-in their task mapping, placement and scheduling algorithms to the framework. In the framework, first energy estimation is calculated based on user configurations and selected components, and the simulated power numbers which including real system activity (traffic scenarios) can make the result be realistic.

The state of the processing element (PE) and the distributed local memory (dual channel as Tx and Rx) demand for each network node can be also observed in real time of the simulation. In this framework, 3D animation for the simulation has been developed, and the link utilization and PE state are included in the animation. Users can obtain a straight view for running the design.

After the simulation, the detailed simulation report which including the overall execution time, throughput, power and energy consumption, link utilizations and the distributed memory demands will be generated automatically by the framework.