





ASVP: The Smart Camera Demo

[SMECY: Smart multicore embedded systems 2010-2013] http://www.smecy.eu

Artemis JU100230 MSMT 7H10001

Control

Data

Data Stream In

Main CPU

Peripherals

Multi-port

Memory

Controlle

DDR

Memor

Data

buffer

Data Stream Out



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BŒ

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FW

FW

Data

Flow

Unit

EW/

ΕW

Data

Flow

Unit

CTRL

local

Merr

CTRL

Loca

Merr

HARDWARE - UTIA ASVP Platform for video processing Application-Specific Vector Processor: Heterogeneous multi-core platform

- System on a chip
 - main CPU, memory controller, peripherals and
- BCE Basic Computing Element (hardware accelerator) Controller with runtime re-programmable firmware
 - Local memories
 - Re-configurable data flow units (1-8 SIMD units)
 - Various computing units
 - (Floating Point/Fixed Point/Integer operations)
- Data transfers
 - Heterogeneous multi-core network with the star topology
 - Batched data transfers
 - Max data transfer rate 2200 MB/s from DDR (2xNPI @ XC5V)



For accelerators based on the UTIA platform

- Compilation Tools PB toolchain
 - Simplified C compiler from firmware in C
 - Linker add API libraries
 - Assembler to PB binary
- Application Programming Interfaces
 - ► WAL Worker Application Layer library unified access to basic computing elements (BCEs)
 - PB2 PB2MB, PB2DFU libraries unified communication with main CPU and DFU
- Simulation Tools
 - Hardware/software co-simulation for architecture analysis
 - Functional simulator for SW development

APPLICATION – Embedded Smart Camera for Video Surveillance

- Process input video stream from camera
- Algorithms for video processing
 - Foreground/background segmentation (motion detection)
 - Opening as morphological noise removal
 - Single-pass object labeling and
- collecting object parameters Implementation
 - In Matlab as reference models
 - In ASVP SoC with a set of hardware accelerators
- Testing of implementation
 - On generated scenes
 - On real testing scenes, in real environment





http://sp.utia.cz

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