eClock

- Easy Clock Generation via All-Digital Phase-Locked Loop (ADPLL) Compiler

You just need steps 1, 2, and 3…

Step 1:
Input Parameters

Step 2:
Search… (~ 5min.)

Step 3:
Output Files

eClock allows you to design your customized ADPLL in minutes…

Our eClock provides you a pure cell-based and all-digital based ADPLL, which has the better noisy immunity and the higher stability as compared to analog ones.

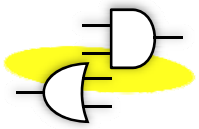
Moreover, eClock can simplify all tasks associated with ADPLL design allowing the user to get a high performance, cost effective design in a much easier way.

By simply selecting a target process technology and defining the reference and output clocks, eClock will search quickly to find one configuration to meet your specification with almost minimum area cost.

Supported Specification of eClock v1.0

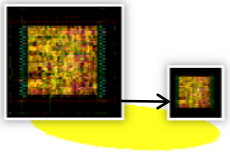
Parameter	Frequency Range	Process		
		0.18um	0.13um	90nm
Maximum Frequency of DCO	F_{max}/F_{min}=1.5	1.64GHz	1.93GHz	4.34GHz
	F_{max}/F_{min}=2.0	1.40GHz	1.74GHz	4.23GHz
	F_{max}/F_{min}=2.5	1.30GHz	1.61GHz	3.84GHz
	F_{max}/F_{min}=3.0	1.09GHz	1.10GHz	3.37GHz

Note: The results are verified with Nanosim in the typical condition.



Easy to Integrate
Use pure standard cell-based architecture.

Easy to Use
eClock can be run through a Graphical User Interface (GUI).



Easy to Migrate
whenever the advanced cell library is ready, it is almost ready.

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