FPGA Prototype of Flexible Heterogeneous multi-ASIP NoC-based Unified Turbo Receiver

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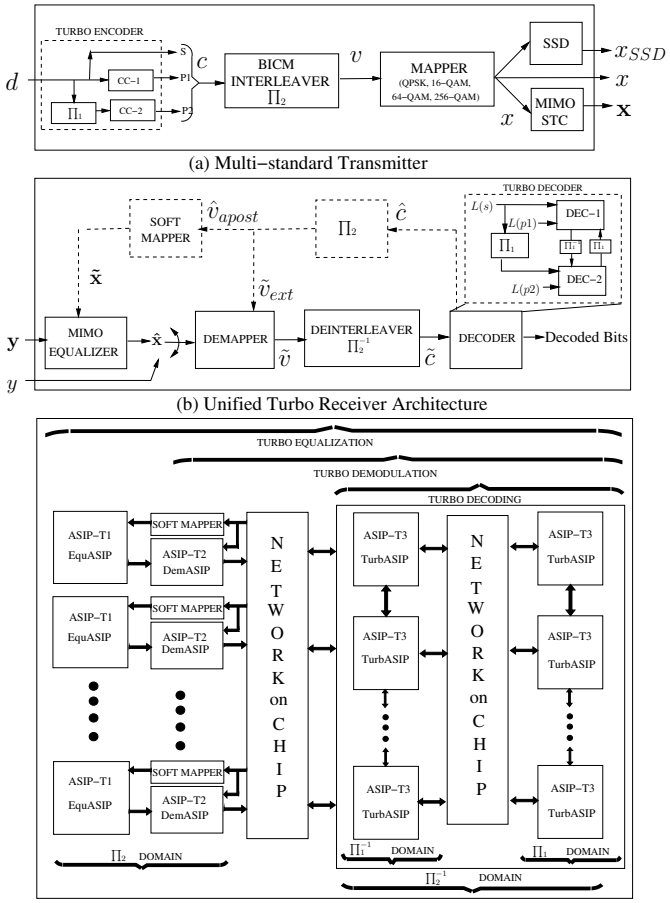
***Abstract*—Recent and emerging wireless standards impose stringent requirements in terms of high throughput, error rate performance and flexibility. Although turbo processing in the receiver ensures error rate performance close to theoretical limits, due to its iterative nature, it creates a bottleneck in achieving high throughput. On the hardware side, the high throughput dedicated architectures can not cope with the flexibility requirements hence some programmable, yet high throughput, architecture is mandatory for future wireless terminals. To address the three stated issues we are demonstrating FPGA prototype of a parallel, flexible and high throughput heterogeneous multi-ASIP NoC-based unified turbo receiver. The proposed prototype can be configured for required parameters by changing application programs of constituent ASIPs and one can extract required processing power by using adequate number of ASIP elements.**

RAPIDLY evolving wireless standards use modern techniques such as turbo codes, Bit Interleaved Coded Modulation (BICM), high order QAM constellation, Signal Space Diversity (SSD) and Multi Input Multi Ouput (MIMO) Space Time Codes (STC) with different parameters for reliable high rate data transmission (Fig. 1(a)). The presented transmitter can impact the receiver architecture in three ways: (1) processing blocks such as turbo codes, encourage to perform iterative processing in the receiver for error rate performance (Fig. 1(b)), (2) to satisfy high throughput requirement for an iterative receiver, parallel processing is mandatory and finally (3) to handle flexibility with high data rate, programmable yet high throughput hardware processing elements are required.

To address the stated requirements, Fig. 1(c) presents a heterogeneous multi-ASIP NoC-based unified turbo receiver. The proposed original architecture uses three types of ASIP dedicated for MIMO MMSE equalization, soft demapping and turbo decoding. Used ASIPs implement efficient parallelism in terms of throughput and flexibility. For further increase in throughput, sub-block parallelism and shuffled decoding (where all constituent blocks of a turbo process execute concurrently) is implemented through multiple instances of heterogeneous ASIPs. These ASIPs process different sub-blocks of a frame in parallel whereas, to handle the communication conflicts due to sub-blocking and shuffled processing Network on Chips (NoC) are used as communication medium.

The overall flexibility of the turbo receiver architecture can be achieved by individual ASIP programming e.g EquASIP for MIMO equalization is flexible for 2×2, 3×3 and 4×4 Spatial Multiplexing (SM), Golden code and Alamouti Code whereas DemASIP can demap any constellation symbol from BPSK to 256-QAM. Finally, TurbASIP can support any 8-state single and double binary turbo code. All three ASIPs can work in iterative context by using *a priori information*. In additions, by switching on/off different ASIPs one can acquire required processing power for a specific application.

In the presented demonstration, a complete communication system is prototyped on FPGA where a transmitter's hardware model implements the architecture presented in Fig. 1(a). Separate hardware channel models are used to emulate single antenna and MIMO Rayleigh fading environment. By



(a) Multi−standard Transmitter

(b) Unified Turbo Receiver Architecture

(c) Heterogeneous multi−ASIP NoC Based Unified Turbo Receiver

Fig. 1. Generic communication system block diagram (a) Multi-standard transmitter, (b) Unified turbo receiver and (c) Heterogeneous multi-ASIP NoC-based unified turbo receiver

integrating 4 instances of each ASIP type and 2 instances of Butterfly topology based NoC, the unified turbo receiver architecture of Fig. 1(c) is conceived. The receiver occupies 56% Slice LUTs, 18% Slice Registers and 37% DSP48E blocks of a Virtex-5 LX330 FPGA with a maximum clock frequency of 135 MHz. For single antenna application, using 2 out of 4 DemASIP and all 4 TurbASIP, the receiver can deliver a throughput of 22 Mbps after 6 shuffled turbo decoding iterations for QPSK modulation whereas with SSD and shuffled turbo demodulation the throughput attains 12.5 Mbps using 4 DemASIP and 4 TurbASIP. For MIMO, with 1 EquASIP, 4 DemASIP and 4 TurbASIP, the throughput is 17.6 Mbps for 2×2 MIMO SM applications in quasi-static channel environment whereas a throughput of 9.6 Mbps with shuffled turbo equalization in block fading channel environment is achieved. Synthesis results targeting a CMOS $90nm$ technology reveal a maximum operating frequency of 512 MHz, and thus a maximum throughput of 4 times that of corresponding FPGA implementation.

REFERENCES

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