Introduction: MTJs are well known as the basic elements of MRAM, a new kind of non-volatile memories which combines high writing/reading speed, low-power consumption, density, hardness to radiations and endurance. Due to this unique set of performances, MTJs can also be used in logic circuits. Although their intrinsic non-volatility naturally encourages using them for memorization purpose, they can also be used to intrinsically mix memory and logic parts of the circuits to push forward the limits of CMOS microelectronics and allow new functionalities. Hybrid CMOS/magnetic technology has the advantage to be easily compatible with the CMOS process: indeed, magnetic devices are realised by adding magnetic and non-magnetic (metal or insulator) layers by post-process above the CMOS layers. To evaluate the performances of such hybrid circuits, it is necessary to be able to integrate these new devices in classical design suites. At transistor level, the design of a logic circuit requires a model of the electrical behaviour of the components and a set of tools to draw and set the layout of the circuit before manufacturing. The work presented here consists in a **full Magnetic Process Design Kit (MPDK)** compatible with Cadence design suite. This PDK is based on the magnetic technology developed in collaboration between CROCUS-Technology and the CEA-LETI. It is graft on the PDK of the hcmos9gp technology from ST Microelectronics. In the first part, we will present the hybrid Magnetic CMOS/Technology. Then, we will describe the MPDK, beginning with the electrical model of the MTJ and moving to the physical verifications tools. At the end, we will illustrate this work by presenting the full design flow for a very simple 1 transistor/1 MTJ memory cell.

MTJ component: MTJ stands for Magnetic Tunnel Junction. A MTJ is a nano-structure basically composed of two Ferro Magnetic (FM) layers separated by an oxide layer (Fig.1). The magnetization of one of the magnetic layer, called hard layer, is pinned and acts as a reference, while the magnetization of the second layer (called soft layer) can be modulated by an external magnetic field, or a current. The resistance of the MTJ depends on the relative magnetization of the two layers (Tunnel Magneto-Resistance, TMR): the resistance at the Parallel state (R_P) is smaller than the resistance at the Anti Parallel state (R_{AP}). The crystalline network and the finite shape of the MTJ result in internal forces, which acts like "internal" magnetic fields and are responsible for the apparition of an "easy" direction in which the magnetization will spontaneously tend to align itself in absence of any external solicitation. For example, if the MTJ has an elliptical section, the magnetization will remain in the largest axis. In practice, for memory applications, the magnetization will have two stable states, Parallel or Anti Parallel to the hard layer, with a hysteretic behaviour. In this case, the value stored in the MTJ is represented by its resistance.

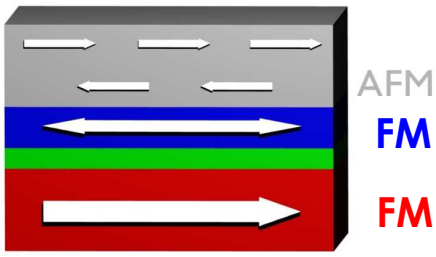

Fig 1: MTJ component

Above IC Magnetic Process: Fig.2 presents the hybrid technology corresponding to the MPDK presented here. The CMOS part is the "hcmos9gp 130nm technology from ST Microelectronics". It contains all the standard process up to the "Metal 5" level including MOS transistors, capacitors, resistors etc. The magnetic part is developed by Crocus-Technology and the CEA-LETI. It contains the MTJ components, connection layers with its dielectrics and additional VIAs to allow connecting the MTJs to the CMOS.

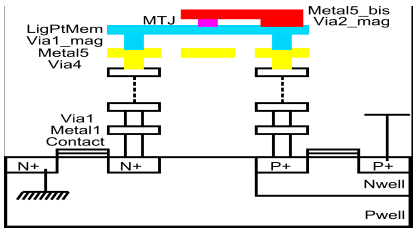

Fig 2: Hybrid technology CMOS / Magnetic

Front End design: An electrical model of the MTJ has been developed. The result is a dynamic library which can be loaded by SPECTRE electrical simulator. The use of this model is very similar to these of the bsim model of the transistor: the model is a generic model of the MTJ, which contains a given number of parameters. Some of these parameters will be chosen independently for each instance. It is typically the case for geometrical parameters (size, shape...). They can be chosen by the designer when he instantiates the devices. The other parameters are linked to the technology and cannot be modified by the designer. The Fig.3 shows the symbol used for the schematic and Fig.4 illustrates the results obtained after simulation.

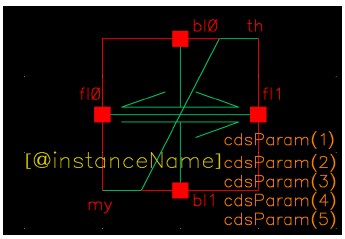

Fig 3: MTJ symbol

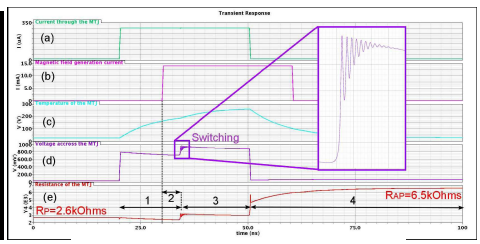

Fig 4: Simulation results

Back End design: Once the correct behaviour of a circuit is checked by simulation, the physical design of the circuit begins. It consists in drawing the layout, that is to say the masks necessary to realize the successive layers of the integrated circuits. The layout has to be checked before being sent for manufacturing. A PDK provides a set of data and tools adapted to a given technology to perform these operations.

- **pCell:** To ease the design, a pCell (parameterized cell) of the components is generally provided by the manufacturer: a pCell is a layout of the device, whose geometry is automatically adapted according to the parameters of the device chosen by the designer, to meet the minimum design rules. This pCell can be easily inserted in the full layout of the circuit. Fig.5 represents the pCell of the MTJ which has been developed for this MPDK.

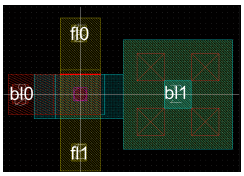

Fig 5: MTJ pCell

- **Verification:** Once the layout is done, the first verification is called **DRC** for Design Rules Checking: it consists in checking if the Design Rules imposed by the manufacturer (minimum width of lines, minimum distance between lines...) are met. These Design Rules are provided in technological files which are part of the PDK. Specific magnetic rules have been implemented in the PDK. The next step is the extraction which consists in identifying the devices and their interconnections from the layout, which is only a set of geometric shapes. The **extraction** operation requires information about the technology, which is also provided in the PDK. After this operation, a netlist of the physical circuit is available. Moreover, since the geometry is now known, it is possible to calculate the parasitic capacitances and resistances of the devices and interconnections, which are added to the netlist and can be used to perform post-layout simulations, taking into account the parasitic devices for more accuracy. The last step consists in checking if the layout corresponds to the circuit which have been simulated. This is the **LVS** (Layout Versus Schematic) step. It consists in comparing the netlists obtained from the schematic and the layout. All these verification tools come with debug tools to help identifying and correcting the errors. The technological files (Design Rules, process parameters) have been modified to integrate the parameters of the magnetic technology, so that all these verifications and debug operations can be performed exactly like for pure CMOS process.

Full design flow example: To illustrate the operation of the MPDK, we will consider the case of a very simple memory cell in TAS technology: Thermally Assisted Switching. The stability of the MTJ when no field is applied is ensured by exchange energy with an additional Anti Ferro Magnetic layer. When a pulse of current is applied through the junction, the temperature increases due to Joule effect. For a temperature above a value called “blocking temperature”, the exchange energy disappears and the junction can be written at lower field. In this case, the selection is partially ensured by heating. This example is composed of a MTJ and a selection transistor to heat it (Fig.6). The circuit required to generate the magnetic field generation current is not presented here. The simulation results for a writing operation is presented Fig.7: (a) represents the voltage applied on the gate of the MOS transistor to generate the heating current, (b) represents the current to generate the magnetic field, (c) the current through the MTJ and (d) the voltage across the MTJ. Due to the variation of resistance of the MTJ, the polarization of the transistor changes during the simulation, resulting in fluctuations of the generated current. The simulation allows choosing the size of the transistor to generate enough current to reach the blocking temperature (150 C) in a given time (10ns). The layout of the cell is given in Fig.8, where we can see the pCell of the MTJ presented previously together with those of a STMicroelectronics MOS transistor. The extraction result is given in Fig.9, where we can see identified components.

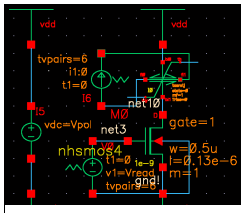

Fig 6: 1T-1MTJ memory cell schematic

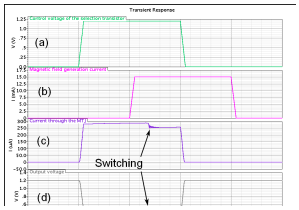

Fig 7: 1T-1MTJ memory cell simulation

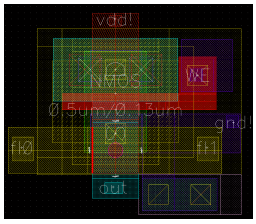

Fig 8: 1T-1MTJ memory cell layout

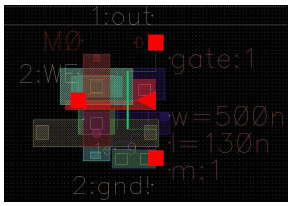

Fig 9: 1T-1MTJ memory cell extracted view

6. CONCLUSIONS

A full hybrid CMOS/Magnetic Process Design Kit was presented. This DK is fully functional for transistor level design of hybrid circuits. It has been used in the framework of research projects to realize demonstrators. The next step of the work will consist in providing the tools required to make pure digital design for more complex circuits. This will require the design of innovative magnetic standard cells and their implementation in the classical digital design flow (digital simulation, synthesis, place and route...)