HDL-based Test Evaluation Tool Set

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***Abstract*— This demonstration provides a test tool set that is based on PLI and VPI interfaces of the Verilog HDL. The tool set includes code coverage analysis, and utilities for evaluation of test and testability methods. The test components provide mechanisms for fault injection, fault simulation, test generation, DFT and BIST evaluation, and test point insertion. A dynamic power estimation tool has also been included in the package for measuring test power. Our tool set includes a netlist generation program that converts EDIF-2 format to proper format for our HDL-based test analysis.**

I. INTRODUCTION

Contentious scaling of the feature size of CMOS technology has resulted in exponential growth in transistor densities, which helps designers to put more functionality on a die. On the other hand, has two unintended manufacturing test related consequences are the increase in test time and the elevated power in test mode. Due to necessity of short time to market, it is desirable to consider testing at the early phases of a design. To cope with this, designers need to have a test framework, compatible with their language. This test framework gives designers some test-related feedbacks and based on these feedbacks they can decide on design and test modifications in the first stages of design. These early modifications reduce time to market.

Furthermore, using the same environment for design and test, all components in a large design can be tested independent of others. In a mixed level design, these advantages make it possible to test a single component described at the gate level, while leaving other components in RTL or even at the system level.

Dynamic power consumption is the dominant part of the test power. We need to estimate the dynamic power consumption during test mode in order to evaluate our test strategy.

In this work, a test tool set has been proposed that takes advantage of PLI and VPI interfaces of Verilog HDL. This tool set can be employed to evaluate DFT insertions and to estimate power consumption of different test methods at during design phase. The interface and Verilog testbench capabilities provide a designer friendly work environment.

II. HDL-BASED TEST PACKAGE

The HDL-based test package includes a netlist generator, PLI test utilities, power estimator and various forms of test applications that are listed here.

A. *Netlist Generators*

Our netlist generator uses the intermediate EDIF-2 format for generating Verilog gate level netlists in a format that is appropriate for our test package utilities.

B. *PLI Test Utilities*

A number of PLI utilities useful for developing test applications are provided in our test package. These utilities include:

- Fault Injection
- Fault Collapsing (Line-oriented)
- Signal Activity Estimator (useful to do statistical fault simulation)
- Module Enabler-Disabler (useful for hierarchical fault simulation)
- Gate-level Walkers
- Controllability and Observability Measurements (SCOAP and Probability-based)

C. *Power Estimator*

We back annotate dynamic power of 2-input gates from transistor level into our generic gate library that has n-input logic gates. Each gate of the design measures its contribution to power and then a PLI function is called at the end to calculate the total test power.

D. *Test Applications*

- Serial Fault Simulation
- Parallel Fault Simulation
- Hierarchical Fault Simulation
- Pseudo Random Test Generation
- Test Data Compaction
- BIST Evaluation
- DFT Evaluation (Virtual Tester)
- Low-power Test Generation
- Test Point Insertion

Figure 1 shows the general form of implementing and running test programs in such a mixed environment.

E. *Code Coverage Analyzer*

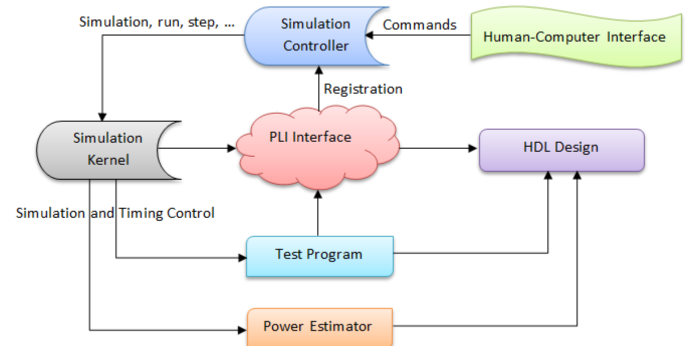

Figure 1 Implementing and running test applications in test environment