Overview

VintAge is a comprehensive solution for the assessment of aging effects in SoC designs.

It consists of a Static Simulation Framework which tracks the aging of data-paths and SRAM memory arrays, and provides accurate estimation of the life-time of processor-based designs.

Easy to integrate into state-of-the-art design tools, VintAge enables the aging characterization of digital circuits at different level of abstraction, from gate level, up to system and application level.

Logic Synthesis & Optimization

application

C-code

HDL

design constraints
F_{ck} – Power – Area

HDL compiler

RTL/gate simulation

VCD

Design Database

Signal Statistics   Memory Access

NBTI Extraction & Annotation

Data-path Analysis

STATIC SIMULATION ENGINE

SRAM Analysis

Timing library

delay characterization

NBTI-aware library

SNM characterization

SRAM

SNM f_{ck}

❖ SoC Operating Frequency Degradation
❖ Register-File and Cache Aging
❖ SoC Lifetime
❖ Effects of Power-Management on Aging

guardband

time

eda group

Politecnico di Torino
C.So Duca degli Abruzzi, 24
10129 Torino - Italy
andrea.calimera@polito.it