Embedded Instruments for Board-level Test

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Abstract

This work introduces a new board-level test technology based on specific synthesizable embedded instruments. The purpose of intelligent embedded instrument is to carry out a vast portion of test application related procedures, perform measurement and configuration of system components thus minimizing the usage of external test equipment. By replacing traditional test and measurement equipment with embedded virtual instruments it is possible not only to achieve the significant reduction of test costs but also facilitate high-speed and at-speed testing.

1. Introduction

During the last decade the evolution of electronic systems has made a major leap. Complex multilayer boards densely stuffed with highly integrated components have become the state of the art in the consumer electronics such as mobile phones, digital cameras, personal computers, etc. On one hand, this trend allows designing "smarter", more compact and power-efficient devices that improve the human's quality of life. On the other hand, it influences in a negative way both the reliability and testability of modern electronic systems.

The electronic manufacturing industry is entering a new age, where static structural test technologies like Boundary Scan (BS) and In-Circuit Test (ICT) start quickly losing their efficiency in terms of fault coverage, while there is currently no existing systematic alternative that can replace them. Despite of constantly improving test automation solutions, the new technological reality elevates the cost of testing in terms of extra engineering efforts and Design-for-Testability (DFT) overhead.

2. State-of-the-art shortcomings

The main problems in the field of system-level testing of complex electronic boards can be summed up as follows:

- Various solutions exist for manufacturing defect testing of complex electronic boards, but all of them have certain limitations (low fault coverage, low speed, expensive equipment). As a result, numerous production test types/test phases have to be used with different test methods applied at every stage, which turns testing into a time-consuming and expensive process.
- Traditional Boundary Scan has shown good diagnostic capability, but is also essentially low speed. Hence the BS test technique has to be complemented by a solution that supports high-speed or at-speed test application mechanisms [1,2] in order to handle dynamic communication protocols like DDR3 or GDDR5.
- Low speed is even more of a problem when it comes to In-System Programming (ISP) where large amounts of data need to be transported over the low speed JTAG port to be programmed into e.g. a Flash memory. With modern industrial examples this procedure typically takes several minutes, but it might require several hours in some specific cases (e.g. flash memories with a serial interface).
- Despite of constantly improving test automation solutions, the new technological reality elevates the cost of testing in terms of extra engineering efforts and Design-for-Testability (DFT) overhead. High costs of test development and equipment in turn elevates manufacturing costs.
- Time-consuming and expensive system-level testing, being a part of the manufacturing process, of every particular instance of an electronic product contributes to high costs of electronics.
- Due to usage of numerous production test types/test phases and a time-consuming testing process, new electronic products need a longer time to reach the market.

3. Proposed Test Architecture

Figure 1 summarises the structure of the proposed target test system. We assume the traditional top-level test access mechanism that is used in JTAG-based testing: the host PC runs test scheduling routines, fetches test data (patterns and control sequences), and sends it through a dedicated test controller to the JTAG port of the system under test (SUT). Here is the point where the progress beyond the state-of-the-art is introduced: instead of the standard JTAG/IEEE1149.1 DFT structures the Host PC communicates with embedded test instrumentation implemented on the FPGA. We assume that SUT contains an FPGA as a part of its design; hence no extra hardware overhead is needed. In the general case, we assume that the embedded instrumentation framework contains a dedicated test processor that is responsible for a fine-grain test scheduling including handling of the target UUT's protocol. The test application is performed using customizable UUT/peripheral controllers to mimic the native UUT interface. In some cases, the test processor can communicate to UUTs via a general purpose I/O (GPIO). In some cases, the test instrumentation can be directly controlled by the Host PC without the use of test

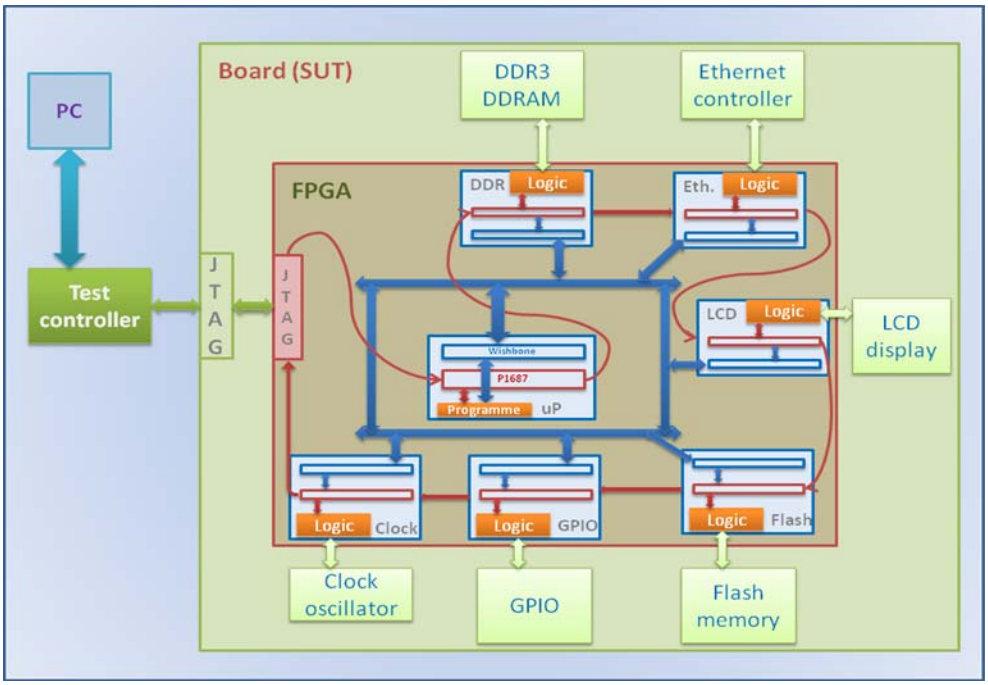

Figure 1. Concept of the proposed test system

processor. Then, the transportation of test data to/from embedded instruments is done via hierarchical JTAG-based structures accordingly to the emerging standards IEEE 1149.7 and IEEE P1687 [3]. We also foresee the trend that many applications currently implemented at the board level will move to 3D integration technology where FPGAs will occupy one or more layers.

4. Embedded Instruments

Although virtual instruments [4,5] gain great attention from researchers and industry, embedded instrumentation is an emerging research area with promising future applications in the industry. There are several important properties/requirements the embedded instrumentation has to fulfil and that make it a very special research topic compared to virtual instrumentation. Virtual instruments are always a part of a fixed hardware platform designed by a measurement equipment vendor as a part of their toolset. Embedded instruments are always being programmed/installed into the UUT itself becoming a "Trojan Horse" that will remove the existing barriers in the test strategy. Since, there is an infinite variety of possible electronic systems in the world, the embedded instruments have to be fully parametrizable and adjustable for the environment they will be placed into. The instruments have to be. The instruments need to be modular, reducible to fit the systems low on programmable resources, thus adaptable to any potential configuration.

5. Conclusions

Intelligent embedded instruments can carry out a vast portion of test application related procedures; perform measurement and configuration of system components thus minimizing the usage of external test equipment. In this case the external tester may only be used for initiating or controlling test execution flow and also for fetching of test results. As a result by replacing traditional test and measurement equipment with embedded virtual instruments it is possible not only to achieve the significant reduction of test costs but also facilitate high-speed and at-speed testing.

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