ATLAS
A Framework for NoC Generation and Evaluation

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MultiProcessor Systems-on-Chip (MPSoCs) are becoming a much more prevalent design style, to achieve tight time-to-market design goals, to maximize design reuse, to simplify the verification process and to provide flexibility and programmability for post-fabrication reuse of complex platforms[8]. Networks-on-chip (NoCs) are the preferable the communication infrastructure to handle MPSoC communication requirements due to its scalability, power efficiency, and support to globally asynchronous locally synchronous (GALS) paradigm [13], [11], [5].

On the other hand, the NoC design - which is composed of cores connected to routers, and routers interconnected by communication channels [4] - is a more complex communication infrastructure than buses. The use of NoCs brings new challenges to the MPSoC design flow such as choosing a suitable routing algorithm, NoC topology, buffering strategy, flow control scheme, or reducing power dissipation. Due to these vast design space alternatives, the automated generation and evaluation of NoCs become a mandatory step in the MPSoCs design flow [11], [3] to establish a good trade-off between the NoC architecture characteristics and the requirements of a given application.

The ATLAS framework automates various processes related to the design flow of some NoCs (such as Hermes [9], Mercury, among others) proposed by the GAPH Group [6] or proposed in collaboration with other groups. Figure 1 presents the design exploration flow of the ATLAS framework.

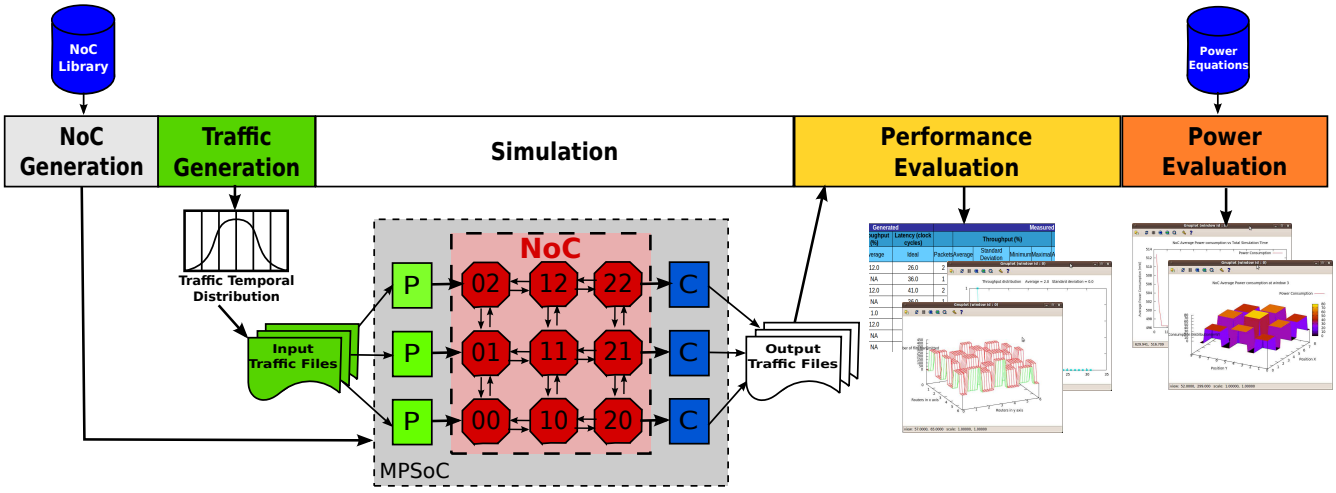

Fig. 1. ATLAS design exploration flow

The ATLAS framework contains the following tools:

1) The **NoC Generation** tool generates the network according to the configuration of following parameters: network dimension; communication channel width; buffer depth; flow control (handshake or credit based); number of virtual channels; scheduling algorithm (round robin or priority); and routing algorithm (XY, west-first, etc). The generated NoC is described in VHDL and its testbenches are described in SystemC.
2) The **Traffic Generation** tool produces different traffic patterns, for different injection rates and source/target pairs (e.g. random and complement). As described in [12], one important concept in traffic modeling is the packet timestamp, which defines the ideal moment that a packet should be inserted into the NoC by a producer (P in Figure 1). The packet timestamp is calculated according different temporal traffic distribution (e.g. normal, uniform and exponential).

3) The **Simulation** tool invokes a external VHDL/SystemC simulator: ModelSim. All generated traffic files are interpreted and injected to the NoC. During the simulation, consumers (C in Figure 1) generate output files that are read by the traffic analysis module, when the simulation finishes, allowing to compute the latency and throughput for each packet.
4) The **Traffic Evaluation** tool verifies if all packets were correctly received, and generates basic statistic data (e.g. a report file and charts) concerning time to deliver packets. The report file presents some traffic analysis results, such as: (*i*) total number of received packets, (*ii*) average time to deliver the packets, (*iii*) total time to deliver all packets and (*iv*) the average, minimal, maximal and standard deviation time to deliver a packet.
5) The **Power Evaluation** tool uses an estimation model [7] to generate NoC power results (e.g. power reports and charts). ATLAS contains a set of predefined equations annotated using a commercial power estimation tool (Synopsys PrimePower). These equations give the energy consumption and power dissipation according to the injection rate at each router port.

The main contribution of the ATLAS framework is to enable the designer to quickly evaluate the performance and power consumption of different NoC configurations, allowing optimize a NoC for a specific application or a set of them. NoCs generated by the ATLAS framework have been successfully prototyped in Xilinx FPGAs and have been used in industrial telecommunication applications [2], [10].

ATLAS is written in Java, allowing its execution in different hardware/software platforms. It also has an intuitive GUI which helps the designer to configure the NoC. The ATLAS framework is an active development project, with contributors and users from different countries, where new features are being included continuously. The latest version of ATLAS is freely available at [1] for download.

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