A dynamically reconfigurable many-core platform for streaming applications

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***Abstract*—Within the Cutting edge Reconfigurable ICs for Stream Processing (CRISP) project, a scalable and dependable reconfigurable many-core system concept has been developed. This concept is demonstrated with a hardware verification board hosting two kinds of chips; the Reconfigurable Fabric Device is used for signal processing, and the General Purpose Device controls the platform. The NOC adapter interface allows for efficient and convenient programming of the 45 XENTIUM® DSP cores. A resource manager abstracts away from the specific locations of the resources, while guaranteeing temporal isolation between processes and dependability information of the various hardware components.**

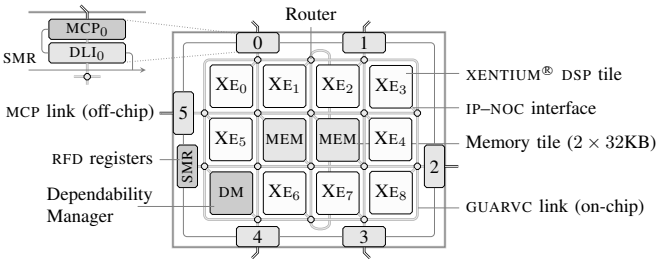

Fig. 1. Reconfigurable Fabric Device

I. Introduction

A. Reconfigurable Fabric Device

The main system constituent is the Reconfigurable Fabric Device (RFD), containing nine XENTIUM® fixed-point DSP cores [1] and two memory tiles. The RFD is manufactured in UMC 90nm CMOS technology, occupying around 44mm^2, and runs at 200 MHZ. Besides the 16 KB data memory and 8 KB instruction cache in the XENTIUM®, localized memory is provided by the memory tiles. Each memory tile combines 64 KB of SRAM (divided in two banks) with flexible address generation units. This allows a datastream to be reordered or the tile to be used as a FIFO. The resources within the RFD are interconnected by a 16-router GUARVC NOC [2] mesh, which in turn is connected to adjacent chips with six MCP ports (see Fig. 1).

B. General Purpose Device

Next to real time computational work, embedded signal processing demands configuration and control. Therefore, the platform incorporates a General Purpose Device (GPD), which is a customized microcontroller [3] with an ARM926EJ–S processing core. The GPD incorporates a GUARVC/MCP adapter for direct NOC access.

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II. Scalable many-core platform

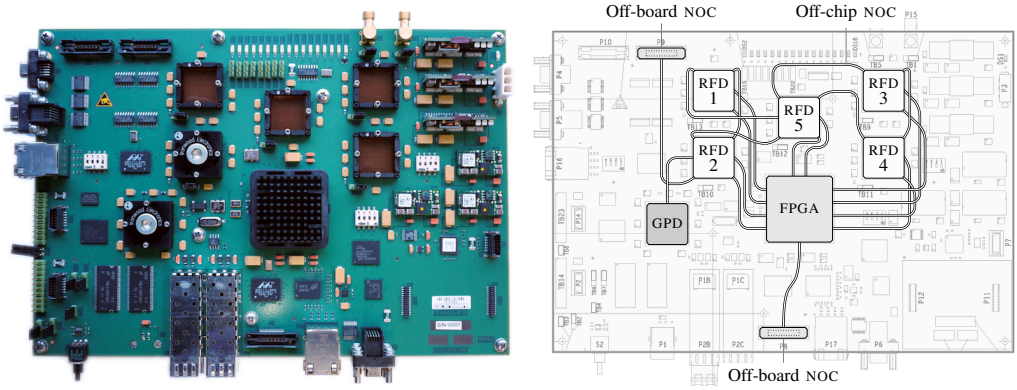
Like the NOC is used to connect all components on-chip, an off-chip network is used to combine RFDs and GPDs into a scalable architecture. MCP ports function as a transparent bridge between the NOCs of different RFDs; optionally, a hierarchical addressing scheme can be used to reduce the routing overhead. With the same technology, multiple boards can be connected together as well, resulting in a heterogeneous hierarchical network of resources. In the CRISP project, a specific configuration of RFDs and GPDs is produced to demonstrate this concept.

A. Hardware verification board

Fig. 2a shows the PCB that is used for the verification of the CRISP concept. Besides the GPD, the board can support up to five RFDs. Fig. 2b identifies the various components mounted on the board. The on-board FPGA serves as a data generator in demonstration scenarios that demand very high data rates, in order to compensate the order of magnitude difference in throughput between on-chip, off-chip and off-board connections.

III. The elegance of the software abstraction

Hardware is only useful if proper software support comes along. The GUARVC NOC protocol is used to transport data through the heterogeneous network. The NOC supports source routing in a packet-switched mode, and provides guaranteed



(a) Hardware verification board

(b) Schematic view showing the various components

Fig. 2. General Stream Processor

services through circuit-switched connections. The user receives a handle to a specific resource on the platform by sending routing information to a device driver. Common file-operations can be used to communicate through this handle with the requested resource. This allows for a rich-featured platform support library that is independent of the specific locations of resources.

A. Run-time resource management

Instead of manually specifying the routing information to a certain type of resource, one may query a higher abstraction layer for resources. Such a resource management layer holds the information about the topology of the platform. Dynamic resource management allows for fault-tolerance in the case that hardware faults can be circumvented, using a disjoint set of resources. However, the amount of resources required by the application does not change. In case that the platform is either seriously compromised, or its available resources are near depletion, applications may be refrained from execution. For robustness reasons, even more flexibility may be added to an application: by providing multiple quality-of-service levels the probability may increase that an application is allowed to start, albeit in a reduced form. This scenario is demonstrated within the CRISP project [4] using the algorithms presented in [5].

The next challenge is to seamlessly switch between the quality-of-service levels provided by an application. Scenarios exists where it is preferred to scale down running applications to allow additional functionality to be performed on the same platform. In other scenarios, hardware faults may trigger a reconfiguration of an application, such that it gracefully degrades by running in a reduced mode on a (slightly) different set of resources.

IV. Demonstration scenarios

Two real-world applications have been developed within the CRISP project; digital beamforming and Global Navigation Satellite System (GNSS) reception [6].

Beamforming is a signal processing technique to transmit or receive data by digitally changing the directionality of an antenna (array). Our beamforming application receives data from 16 antennas (generated by the FPGA), and requires all five RFDs to extract 8 output beams at a rate of 640 Mbps.

The GNSS application can aquire and track satellites using GPS, by matching the number of XENTIUM® cores required to the availability of satellite data. This application can be considered as a consumer type of application, typically requiring only a subset of resources of a single RFD.

A. Dependability Manager

Next to running 'normal' applications, system test and monitoring applications can be run alongside, using the unique dependability features of the hardware platform. Fig. 1 shows the Dependability Manager, which is used to perform BIST and scan chain tests simultaneously using up to three XENTIUM® cores [7]. The demonstration includes running the GNSS application together with some dependability tests.

References

[1] Recore Systems. (2011, Jan.) Reconfigurable computing technology. [Online]. Available: http://www.recoresystems.com/technology/

[2] P. T. Wolkotte, "Exploration within the network-on-chip paradigm," Ph.D. dissertation, University of Twente, 2009.

[3] Atmel. (2009, Mar.) AT91CAP9S250A customizable microcontroller processor. [Online]. Available: http://www.atmel.com/dyn/resources/prod_documents/doc6264.pdf

[4] The CRISP Consortium. (2011, Jan.) CRISP - Cutting edge Reconfigurable ICs for Stream Processing. FP7-ICT-215881. [Online]. Available: http://www.crisp-project.eu

[5] T. D. ter Braak, P. K. F. Hölzenspies, J. Kuper, J. L. Hurink, and G. J. M. Smit, "Run-time spatial resource management for real-time applications on heterogeneous mpsocs," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE 2010), Dresden*. European Design and Automation Association, March 2010, pp. 357–362.

[6] H. Hurskainen, J. Raasakka, T. Ahonen, and J. Nurmi, "Multicore software-defined radio architecture for gnss receiver signal processing," *EURASIP J. Embedded Syst.*, vol. 2009, pp. 3:1–3:10, January 2009. [Online]. Available: http://dx.doi.org/10.1155/2009/543720

[7] H. G. Kerkhoff and X. Zhang, "Design of an infrastructural ip dependability manager for a dependable reconfigurable many-core processor," in *Fifth IEEE International Symposium on Electronic Design, Test & Applications, DELTA 2010, Ho Chi Minh City, Vietnam*. Los Alamitos, CA: IEEE Computer Society Press, January 2010, pp. 270–275.