IdEM & MπLOG: MACROMODELING TOOLS FOR SYSTEM-LEVEL SIGNAL INTEGRITY AND EMC ASSESSMENT

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Abstract

IdEM and Mπlog are CAD tools for passive model extraction of interconnects and behavioral description of digital IO buffers, respectively. Both technologies generate SPICE models enabling fast and accurate mixed-signal design.

1. Introduction

The complexity of modern high-end electronic systems as well as strict time-to-market constraints require fast and reliable Signal Integrity and Electromagnetic Compatibility performance assessments since very preliminary stages of the design. Such assessments are usually performed via numerical simulations aimed at the prediction of the signals propagating on the system interconnects. This type of analysis is enabled by the availability of accurate and efficient models for all relevant system components including, e.g., interconnects, vias, connectors, packages, discontinuities, as well as digital integrated circuits (ICs) output (drivers) and input (receivers) ports.
Within this framework, the research activity carried out by the EMC group at the Politecnico di Torino focuses on the development of a set of CAD tools for the generation of both device and interconnect macromodels [1]. The state-of-the-art modeling algorithms [2-4] that are continuously developed as a research task are embedded in Matlab-based user-friendly graphical interfaces, allowing a step-by-step generation of models. A brief overview of the two main tools (available from the official website of the research group [1]) is reported below.

2. IdEM: Macromodeling of Linear Interconnects

IdEM stands for Identification of Electrical Macromodels. It is aimed at the generation of macromodels for linear lumped multiport structures (e.g., connectors, packages, vias, discontinuities, ...), known from their input-output port responses [1]. The input-output characterization of the structure under investigation can come from measurement or simulation, either in frequency domain or in time domain. IdEM uses state-of-the-art fitting algorithms for rational approximations, based on various formulations of the Vector Fitting scheme and includes an efficient passivity check and compensation of macromodels [2,3]. In addition, several import filters are available for common data formats. A SPICE link allows the automatic synthesis of the macromodels into equivalent circuits that can be processed by standard circuit solvers. Figure 1 collects the main steps provided by the IdEM tool for the generation of interconnect macromodels.

3. Mπlog: Macromodeling of Digital I/O Ports

Mπlog (Macromodeling via Parametric Identification of LOgic Gates) is a tool designed for the interactive generation of macromodels for the I/O ports of digital integrated circuits [1,4]. The proposed models are mathematical relations approximating the port electrical behavior of devices, thus completely hiding the internal structure of devices and preserving the proprietary information of vendors. The models are derived via advanced identification algorithms from transient port responses, which can be obtained via direct measurements or transistor-level circuit simulation. The model accuracy is superior to current industrial standards, and the model complexity is negligible with respect to transistor-level models of the devices. The models can be implemented in several formats as SPICE subcircuits to be directly included in most commercial simulators. Figure 2 shows the step-by-step procedure for the model generation provided by the Mπlog tool.

4. References

[1] Tools and documentation downloadable from the official EMC Group website http://www.emc.polito.it.
[2] F. G. Canavero, S. Grivet-Talocia, I. A. Maio, I. S. Stievano, "Linear and Nonlinear Macromodels for System-Level Signal Integrity and EMC Assessment" , *IEICE Transactions on Communications - Special Issue on EMC,* pp. Vol. E88-B, No. 8, August, 2005.
[3] S. Grivet-Talocia, "Passivity Enforcement via Perturbation of Hamiltonian Matrices" , *IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications*, pp. 1755-1769, vol. 51, n. 9, September, 2004.
[4] I. S. Stievano, I. A. Maio, F. G. Canavero, "M[pi]log, Macromodeling via Parametric Identification of Logic Gates", *IEEE Transactions on Advanced Packaging*, pp. 15-23, vol. 27, n. 2, February, 2004.

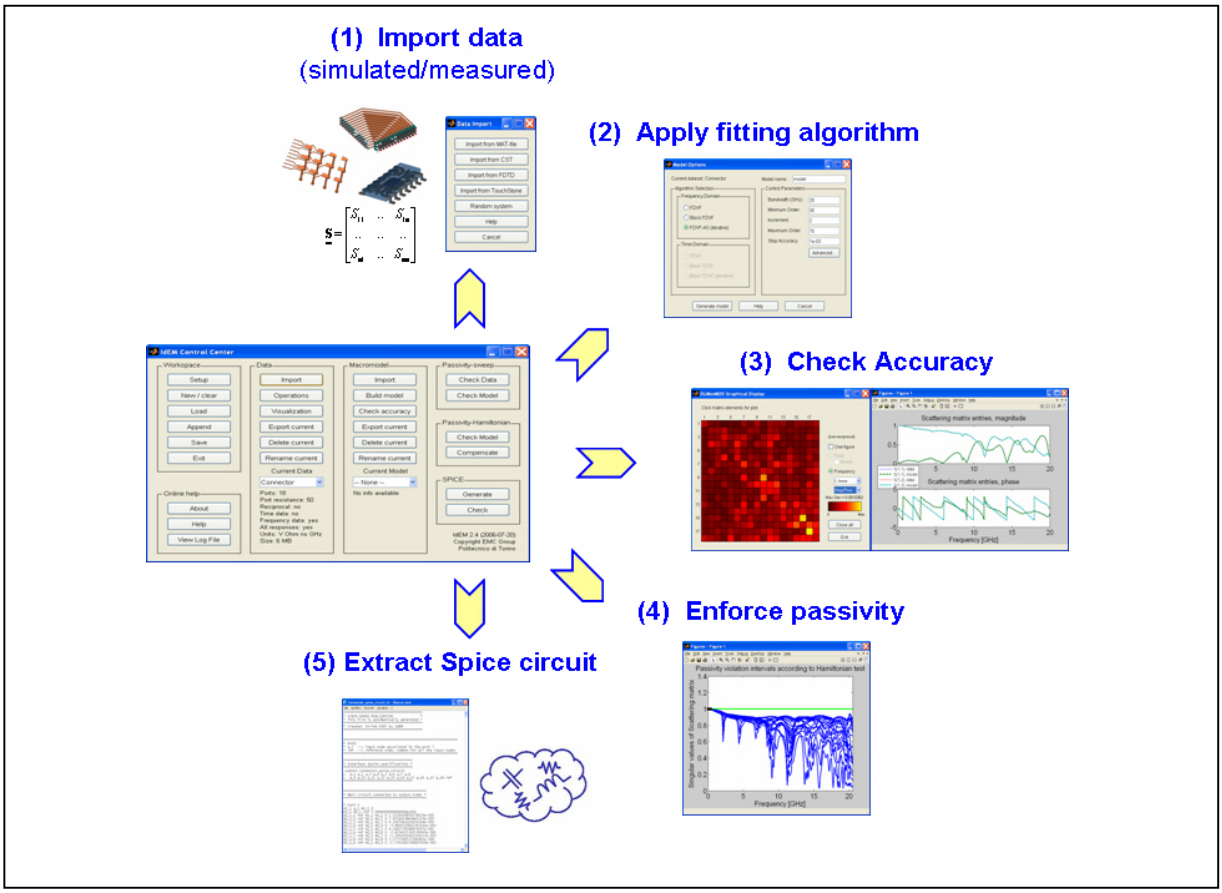

Figure 1: Step-by step procedure for the generation of interconnect macromodels via IdEM.

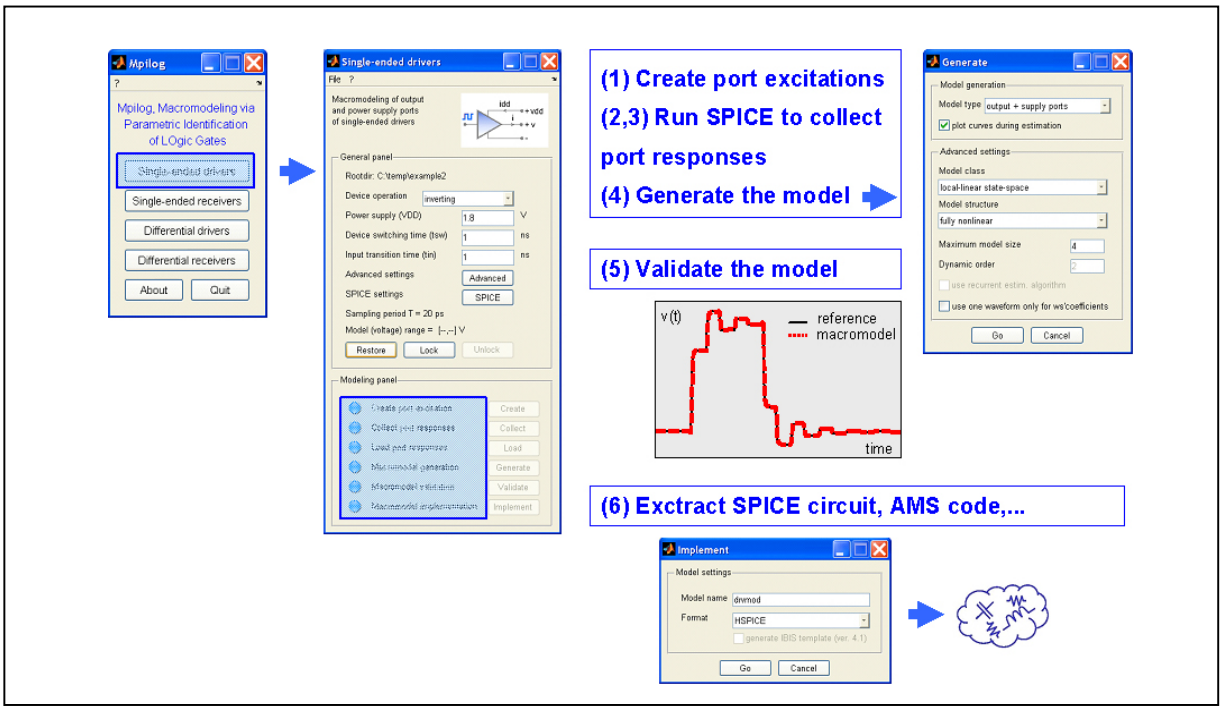

Figure 2: Step-by step procedure for the generation of device macromodels via Mπlog.