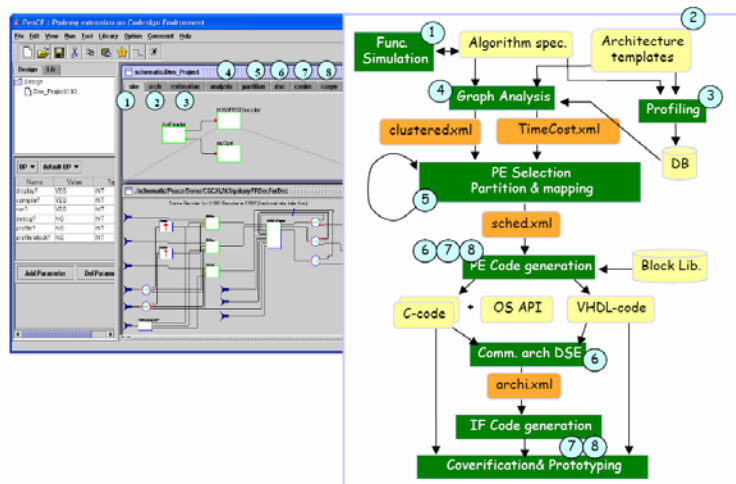PeaCE 1.0.1 functionality description

1. System Specification and Functional Simulation ①

   PeaCE provides system-level specification of a complicated system like H.264 using task model/SDF/fFSM.

2. Architecture Selection ②

   PeaCE supports two types of architecture specification: one for specifying an existent platform architecture, and the other for generating a customized architecture tailored to the given application.

3. Performance Estimation and Graph Analysis ③④

   PeaCE analyzes bock dependency and estimates the block execution time on the candidate processing elements.

4. Automatic/Manual Partitioning ⑤

   PeaCE supports not only automatic HW/SW partitioning but also manual partitioning capability for a given architecture model.

5. On-Chip Bus Architecture Refinement ⑥

   PeaCE explores the optimal bus architecture to meet the performance requirements.

6. Cosimulation and Profiling ⑦

   PeaCE performs HW/SW cosimulation for performance verification using virtual synchronization technique.

7. HW/SW Cosynthesis and Interface Generation ⑧

   The system specification is partitioned into sub-graphs for a software and a hardware. PeaCE generates C code for SW and VHDL code for HW.

8. Coverification using SeamlessCVE^{TM} ⑧

   PeaCE automatically generates, compiles, and builds RTL code for the top-level entity of the platform as well as system components and invokes SeamlessCVE^{TM} for co-verification.