

The IEEE 1500 standard addresses the specific challenges that come with testing deeply embedded reusable cores supplied by diverse providers, who often use different hardware description levels and mixed technologies.

A 1500 architecture always includes:

- *A Core Test Wrapper*: a wrapper placed around the boundaries of the core that allows accessing the testing functionalities of the core using a standard interface and protocol.
- *An Information Model*: the formal description of the functionalities of the P1500 wrapper of the core. The 1500 standard includes many functionalities, some being optional. The Information Model is the link between core providers and core users and facilitates the integration of the core with the rest of the design. The Information Model is described in the *Core Test Language (CTL)*.

IEEE 1500 allows two different levels of compliance:

- **IEEE 1500 Compliant Core**: this notion refers to a core that incorporates an IEEE 1500 wrapper function, and comes with the related CTL file. The CTL file describes the core test knowledge, including how to operate the wrapper, at the wrapper's external terminals.
- **IEEE 1500 Ready Core**: this notion refers to a core which does not have a complete IEEE 1500 wrapper, but does have a CTL file on the basis of which the core could be made '1500-Compliant', either manually or by using dedicated tools. The CTL file describes the core test knowledge at the bare core terminals.

In this scenery, if the use of a standard as the P1500 is very important, even more important it is the availability of a tool to check whether a core is P1500-Compliant, or not. The 1500 Compliance Checking Tool (1500 CCE) is a design environment to verify the system core-wrapper 1500-Compliance with the purpose to assure that the component can be successfully integrated in a SoC. In addition, the tool can assist the core suppliers in providing a CTL description of the core, create the CTL description of a 1500-Compliant wrapper for the unwrapped core, synthesize the relative VHDL wrapper, and suit the core test patterns for the wrapper.