Automated Hierarchical Knowledge-Based Synthesis for Analog Cells using CAIRO+

Ramy Iskander, P. Nguyen Tuong, L. de Lamarre, V. Bourguet, M.-M. Louërat and A. Greiner

University of Pierre et Marie Curie, Paris VI,
LIP6 Laboratory,
4, Place Jussieu, 75252 Paris, France
Email : ramy.iskander@lip6.fr

Here we present the CAIRO+ language [1, 2] that allows the analog designer to create parameterized generators of analog functions. CAIRO+ is aimed to help the designer to document his knowledge thus creating a library of analog functions. Complex hierarchical analog function generators are designed by using existing generators of simpler functions. These generators can be designed to be independent of the fabrication process thus enabling process and specification migration. The CAIRO+ language, composed of C++ predefined functions, is a new answer to the automation of electrical and layout design of analog circuits [3].
CAIRO+ operates in two different modes : *design* and *synthesis*. In the *design* mode, the designer defines hierarchy and provides suitable sizing and biasing procedure for the analog cell. A sizing and biasing procedure is a routine that computes the sizes and biasing voltages for a transistor. The designer also controls electrical parameter propagation between different modules and devices in the hierarchy. In the *synthesis* mode, the designer defines the hierarchy and provides some basic electrical parameters about devices. Integrity checks are enforced to ensure electrical coherence for devices. The sizing and biasing procedure is automatically extracted from the hierarchy and executed to size and bias the whole cell.
In order to design a new module generator, the analog designer has to write the following functions corresponding to our design flow :

1. **Capture of Netlist and Layout Templates.** In this step, functions allow the creation of the netlist and the relative placement of unsized instances.
2. **Design Space Exploration.** In the *design* mode [4], specifications are propagated from top to down in the module tree thanks to dedicated functions used by the designer to develop his own sizing strategy. The result is a sized schematic. In the *synthesis* mode [5], a sizing and biasing procedure is automatically extracted based on the hierarchy of the analog cell. The extracted procedure is then executed to determine all electrical and small signal parameters of each transistor in the circuit. Automatic offset voltages are inserted in the cell to ensure that all user conditions are respected in the case of well-constrained, under-constrained and over-constrained transistors.
3. **Procedural Routing.** During this step, the designer routes the cell using predefined routing functions. These functions ensures correct routing for any device shape deformation during synthesis.

Finally, given a geometrical constraint, like module height or aspect ratio, the feasible height of the module is selected, by examining it's shape function. With a recursive top to bottom approach, the actual shape of devices is selected. Then the relative placement is performed. Hierarchical routing from bottom to top is then performed.

RÉFÉRENCES

[1] Pierre Nguyen Tuong, Marie-Minerve Rosset-Louerat, and Alain Greiner. Guidelines for Designing Smart and Reusable Analog IP Cores. *Proc. Sophia Antipolis MicroElectronics Forum (SAME)*, 2004.

[2] Vincent Bourguet, Laurent de Lamarre, and Marie-Minerve Rosset-Louerat. Analog IC Design with a Library of Parameterized Device Generators. *Proc. XIX Conference on Design of Circuits and Integrated Systems (DCIS)*, 2004.

[3] Mohamed Dessouky, Marie-Minerve Louërat, and Jacky Porte. Layout-Oriented Synthesis of High Performance Analog Circuits. *Proc. Design, Automation and Test in Europe (DATE)*, pages 53–57, 2000.

[4] Ramy Iskander, Laurent de Lamarre, Andreas Kaiser, and Marie-Minerve Rosset-Louerat. Design Space Exploration for Analog IPs using CAIRO+. *Proc. The International Conference on Electrical Electronic and Computer Engineering*, pages 473–476, 2004.

[5] Ramy Iskander, Andreas Kaiser, and Marie-Minerve Louerat. Automatic Biasing Point Extraction and Design Plan Generation for Analog IPs. *Proc. The 48th IEEE MidWest Symposium on Circuits And Systems*, 2005.