Yield Estimation Tool Considering Via Failures

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Abstract

We can estimate the total number of vias in a circuit, which is derived from a gate-level netlist(Verilog, etc) instead of layout. The total number of vias depends on the yield of a circuit. We can estimate the yield considering via failures with this tool.

A part of this work was presented in DATE' 2004 and will be presented in ISQED' 2006.

Estimation Flow Figure 1 shows the procedure to estimate the total number of vias. The total number of vias is calculated using the wire-length distribution [1] and the via distribution [2]. The wire-length distribution is derived from a gate-level netlist and the via distribution is derived from track utilization and the model parameters: α, β. The model parameters depends on the routing algorithm and the geometric structure. The model parameters are extracted from the previously-designed circuits, which are stored as data base. The data base has the number of vias per net, track utilization, the routing algorithm, and the geometric structure. The extracted model parameters can be used for the same process and the same routing tool. Yield is estimated using the failure rate of each via, the via distribution, and the wire-length distribution. The total number of vias $n_{\rm total}$ is calculated as a product of the via distribution and the wire-length distribution. The yield considering via defects is calculated as follows.

$$y_{ield} = (1-\lambda)^{n_{\rm total}} \tag{1}$$

where λ is failure rate of via, and $n_{\rm total}$ is the total number of vias in a circuit.

Via Distribution Model The number of vias on a wire has large dependence on the number of detours. The longer wire has more vias due to the increase of the number of detours, and the longer wire also uses more vias to use upper metal layers. In this paper, the relationship between the wire length and the number of vias is statistically modeled as an exponential function.

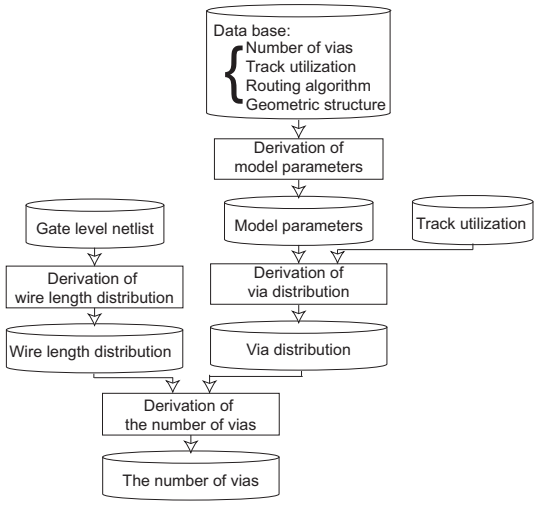

Figure 1. Flow to estimate the total number of vias.

$$n_{\rm via}(\ell) = \alpha \ell^{\beta}, \tag{2}$$

where ℓ is the wire length, and n_{via} is the number of vias on a wire.

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References

[1] J. A. Davis, *et al.*, *IEEE Trans. on Electron Devices*, Vol. 45, No. 3, pp. 580–589, 1998.

[2] T. Uezono, *et al.*, to be presented at *International Symposium on Quality Electronic Design*, 2006.