A High-Level Synthesis Tool for the MACT Architecture

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Abstract

The growing need for application class specific but still flexible data processing leads to a demand of new computer architectures. Reorganziation and combination of proven design paradigms are promising ways to reach these goals. The fully re-configurable self-timed bit-serial and fully interlocked MACT architecture is one of those new architectures. Although MACT does not rely on a central controller, its local synchronization still demands special care is taken. This fact is especially true if routers are added to the architecture. To support all features of MACT a new High-Level Synthesis tool is required.

The tool, we call it MHLS (MACT High-Level Synthesis), starts with the scheduling phase of the dataflow graph. Due to the bit-serial characteristic of MACT the allocation and binding phase is simple, because all operations within the dataflow graph are directly mapped to real resources. Furthermore, all additional control wires of MACT are generated during the synthesis. Figure 1 shows a screenshot of the MHLS tool. In the upper of the figure, we can see the graphical input window. Here the user can draw the dataflow graph with the help of basic operations provided by the tool. This basic operations stored in a library can easily be extended by the user. Besides the graphical input it is also possible to use the textual interface. Therefore, a grammar is defined. An extension to generate the dataflow graph from a hardware description language (HDL) like SystemC is right now under development. Additional information during the synthesis process of the design are displayed in the console window.

High speed, parallelism, re-programmability and compactness are the main characteristics of MACT and vital for the realization of embedded systems. As an application example, we present an image processing on the Celoxica RC 200 board.

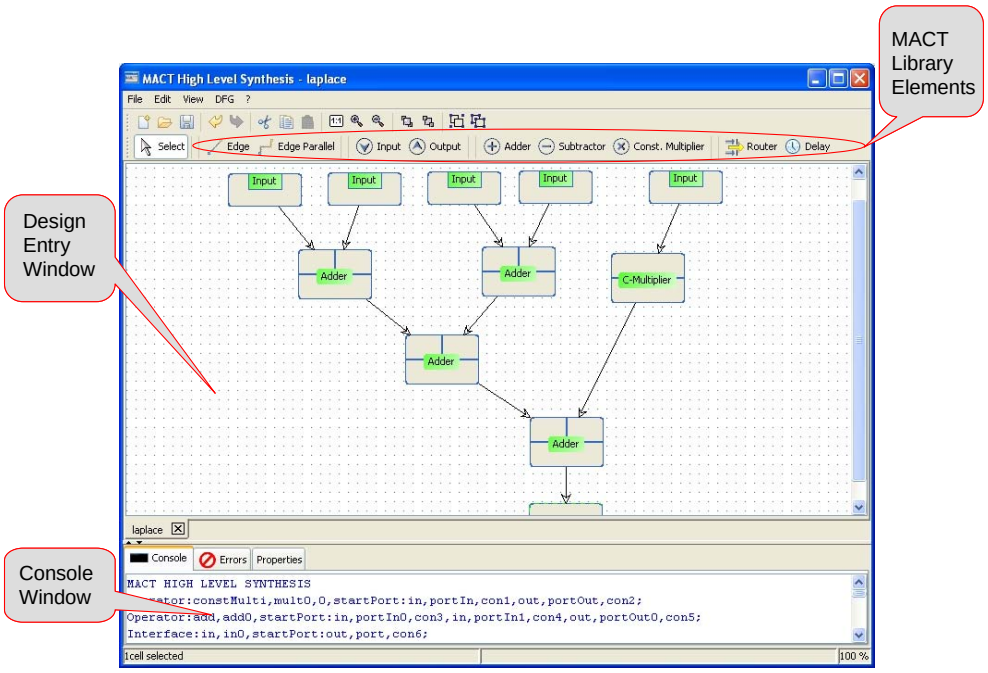

Figure 1: The MACT High-Level Synthesis tool – MHLS