

1 STEAC

With the increasing size and complexity of advanced VLSI design, the integration of heterogeneous cores from different sources into a system-on-chip (SOC) brings new challenges not only on the design phase but also on the test one. In figure 1(a), STEAC (SOC TEST Aid Console) provides an SOC test integration platform which can automatically do the SOC test scheduling, test circuit insertion and system-level pattern translation by setting an easy TestSpec file which specifies the IP test information and HDL design with DFT information. We propose the Test Access Control System (TACS) as the SOC test integration solution. Figure 1(b) shows the test architecture of TACS. Based on the IEEE 1500 test wrapper, a flexible test access mechanism (TAM) and the associated test controller are developed. The TACS reuses the IEEE 1149.1 Test Access Port (TAP) interface for test control with small pin and area overhead. STEAC is developed based on IEEE 1450 Standard Test Interface Language (STIL) and 1450.6 Core Test Language (CTL) to facilitate the test integration process, while it outputs a netlist with the proposed test architecture and the associated system-level test patterns in standard HDL format. With the help of STEAC, fast test time evaluation, easy test architecture insertion and precise test pattern translation can be done easily.

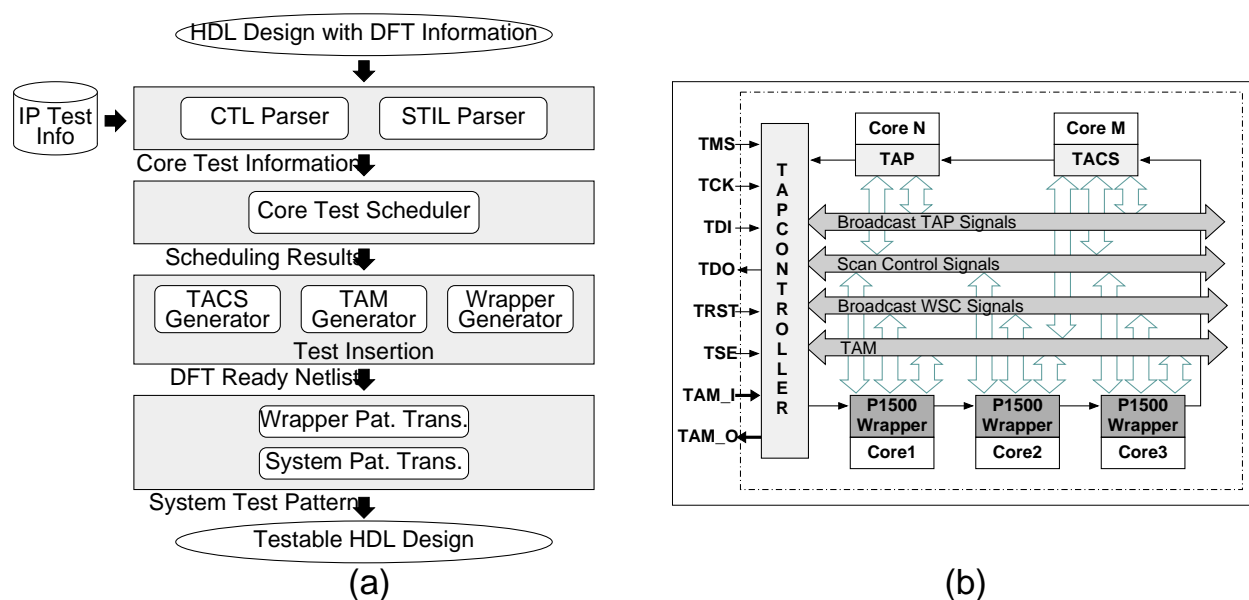


Figure 1: (a)SOC test integration flow of STEAC and (b)Test architecture of TACS.