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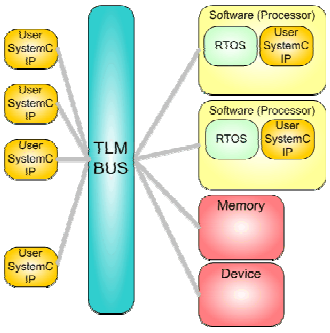
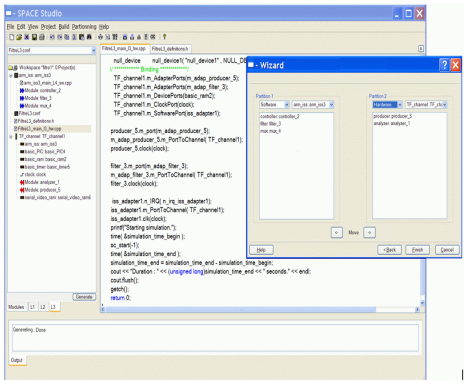
Designing SoC/FPGA at High-Level

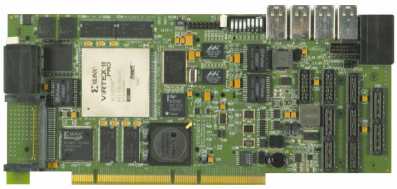


Technology advances have a tremendous effect on the complexity of chips. To enhance productivity in the fields of design and simulation of systems on chips, higher levels of abstraction have been defined. Description languages must handle both hardware and software components as well as be able to capture systems constraints and describe their communication. For instance, the designer productivity can be greatly improved using a transactional level model that abstracts the functionalities of the system being designed. To answer this abstraction issue, the concept of virtual platform has been proposed. A lot of work has been accomplished to support efficient Hw/Sw (Hardware/Software) partitioning that maps a functional specification onto such virtual platforms. No commercial solution provides a complete methodology including a support of embedded software for heterogeneous systems and Hw/Sw real architectural exploration.



SPACE Codesign is a SystemC virtual platform toolset that enables simulation and performance assessment at the transactional level. The platform also facilitates modeling of multiprocessing embedded systems, RTOS efficient integration into simulations, architectural exploration, and a refinement process to implement physically on FPGA (SoC) the best Hw/Sw solution obtained through automated partitioning. Moreover, a Hw/Sw automated co-synthesis approach ensure an automatic translation between SystemC design using the SPACE Codesign toolset and FPGA implementation tools.

Finally, we discuss about our approach to bring up SPACE Codesign from a research project towards a commercial solution in order to facilitate its commercialization: first, by looking on the development of SoC applications using SPACE Codesign which will be used to support first sales and second by increasing the functionality of SPACE Codesign.



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