PART-E

In the field of FPGA design, a tool is presented that focuses on the partial run-time reconfiguration capability. The tool automates the generation of bitstreams. Its front-end is realized in the Eclipse environment. It provides several views of the design that are specified to visualize the temporal and spatial domains of reconfigurable systems.

The possibility of partial reconfiguration of FPGAs during run-time can be used to implement systems that adapt their execution area over time, e. g., achieving resource optimization. However, systems that exploit (run-time) reconfiguration are still rarely found. One reason is the missing tool support, which would open reconfigurable computing to a broader audience by automating hand work and abstracting away cumbersome design details.

Easing Partial Bitstream Generation

We present a tool that meets this requirement. It was developed to ease the design of partial bitstreams for Xilinx FPGAs for research purpose. Primarily, the tool wraps the obstacles of partial bitstream generation. Furthermore, the tool extends the pure generation of bitstreams by several additional features that ease the design of reconfigurable systems. Thus, the tool can be used to directly generate partial bit-streams for FPGAs, as well as explore different design alternatives of partial reconfigurable systems.

Eclipse Framework

For convenience, the tool is based on the Eclipse environment as a Plug-In. The Eclipse environment is a well-know framework initially designed for Java development, and is increasingly used in different design processes including the embedded field. Thus, users that are familiar with Eclipse can easily feel comfortable with the tool, while EDA designers can rely on the standardized design of the framework for maintainability purposes. Moreover, as Eclipse's intention is to ease the user specific design flow and not to guide through a design process on an exclusive path, the tool is open for multiple purposes. Users can select different views of the design/project. Having multiple different angles to the same problem is most beneficial for the design of reconfigurable systems. Eclipse suits the needs for such a design process. Thus, designers can view the time and space axes for reconfigurable systems.

Abstraction Using UML

Moreover, the backend of the tool, a single UML class diagram that represents the whole characteristics of the reconfigurable system under development abstractly, allows to model reconfigurable systems in a comprehensive manner on a high level of abstraction. The UML diagram is filled during the design process until enough information for the generation of bitstreams is available. Thus, it serves as possibility to explore the dependencies as well as the versatility of reconfigurable systems.

The Tool PART-E

We present our tool PART-E that was developed to provide an integrated means of designing partially reconfigurable systems, including the generation of partial bitstreams. The tool was implemented relying on one single model as backbone. All design explorations are performed on this single model. Thus, we can eases the design process despite the complexity of partially reconfigurable systems.
The tool enables to combine HDL-Modules, which each represent a task to be executed dynamically on the FPGA, to so-called Tops, which assemble and structure the design including global logic, etc. Each Top comprises the set of Modules that can be present on an FPGA at the same time. Additionally, physical constraints like the position of the tasks on the FPGA are necessary. The tool eases the generation of those physical constraints, including the placement of inter-module connections. The properties are displayed in the several views, all referring to the same model. Finally, the integrated call of automatically generated commands following the Xilinx application note 290 enables the convenient generation and download of the partial and full bitstreams.

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