The ODYSSEY System-Level Design Tool Description

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We demonstrate an ESL design tool that implements an Object-Oriented (OO) C++ application as collaborating hardware and software components on a VirtexII-Pro FPGA.

The design flow starts from OO C++ source code and is composed of two stages. In the upper stage (labelled "System-Level Synthesis" in Fig. 1), the design is parsed and analysed and the hardware-software partitioning decision is made. The unit of assigning functionality to hardware and software is *a method of a class*. Automatic partitioning is not yet supported by the tool but the tool is capable of implementing any desired partitioning. At the end of this first stage, an executable hardware-software co-simulation model is generated in SystemC that models the final implementation at transaction level. This Transaction-Level Model (TLM) serves as an efficient verification checkpoint before starting the lower stage of the design flow (labelled "Downstream Synthesis" in Fig. 1) that involves several time-consuming and intricate tasks for behavioural synthesis of the hardware units and for compilation of software parts. At the end of this stage, a bitstream is generated to configure a Xilinx VirtexII-Pro FPGA.

Our tool provides a complete path from untimed OO C++ application to working FPGA although some decision-makings are still manual. Two major software abstractions, namely inheritance and polymorphism (including virtual-method despatch to and from in-hardware and in-software methods), are fully supported by the tool and implemented in the final system. The executable co-simulation model is another advantage of the tool that enables the designer to gain orders of magnitude co-simulation speedup compared to final gate-level simulation so as to apply more stimuli at less time.

We have developed a number of case studies including JPEG and MPEG2 decoders using our tool and methodology. At the time of submitting this description, these case studies are fully implemented and verified by simulation. The team is now working on completing the design flow by demonstrating the case studies on a Xilinx development board we have just obtained. This is anticipated to get finished before DATE'06 conference and we wish to demonstrate the entire design flow from OO C++ to working implementation on an FPGA board in the University Booth.

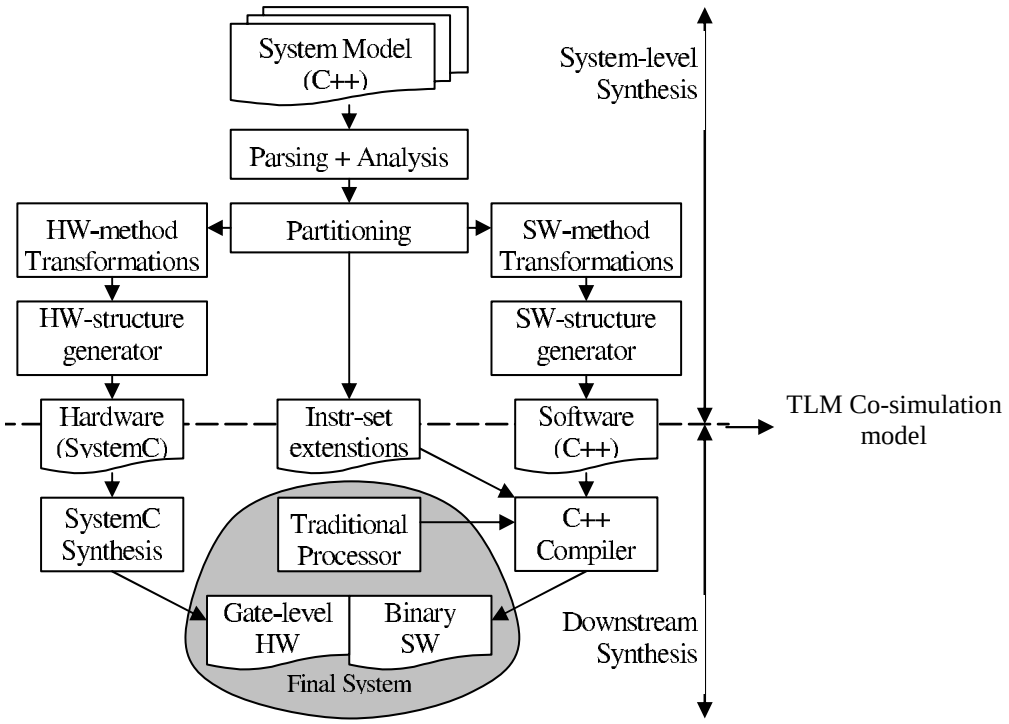

Figure 1. Big picture of the internal operations of the tool.