Multiple simultaneous upset fault-tolerant FIR circuit design using delta-sigma modulation

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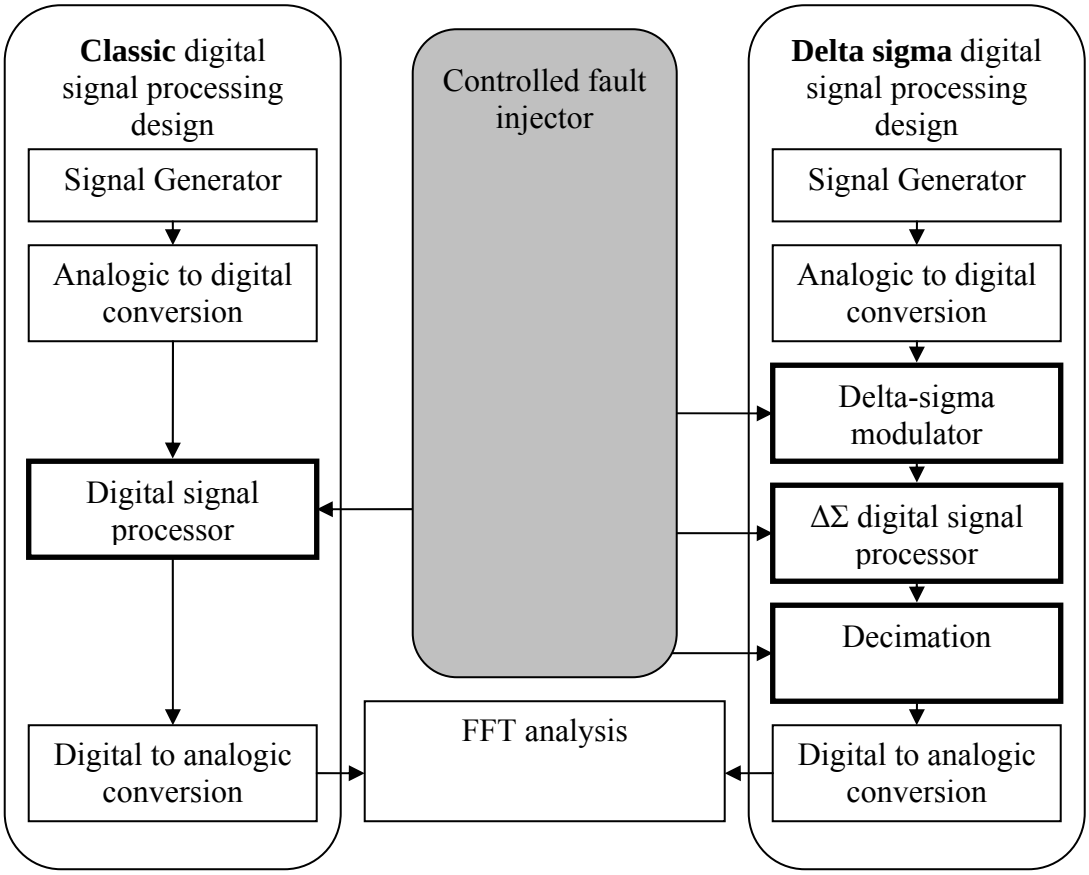
We have proved the efficacy of delta-sigma modulation to increase fault-tolerant characteristics of circuits. To demonstrate this theoretical and simulation results, it was built two circuits implementing digital FIR filters with controlled fault injection. Although both present similar functionality, the first one is designed to modulate the signal with delta-sigma modulation and filter it with a specific structure.

The figure below exhibit the overall scheme for the demonstration:



The analog to digital conversion blocks are placed in a specially projected board, but the digital blocks are implemented with a design kit constituted by a FPGA. The possibility of compiling the digital blocks in the same chip provides reports of area occupation by the synthesizer software.

With the controlled fault injection we can vary the amount of faults and follow the corresponding signal degradation. Since both systems are running in parallel, we can compare their fault tolerance capabilities in real-time through the *fast fourier transform* (FFT) of both signals.

The comparison states the delta-sigma modulator as a better scheme for fault-tolerant systems design than the classic design and may be used for many critical applications where multiple and/or simultaneous faults occur.