1 BRAINS

BRAINS (Bist for RAm IN Seconds) is a framework for embedded memory built-in self-test (BIST) compilation, and it supports common memory architectures. According to the memory specifications and the test requirements, BRAINS generates the synthesizable BIST code in Verilog HDL, as well as its activation sequence, test bench and synthesis scripts. These can help user to validate the BIST function by logic simulation and to adjust the BIST timing for different fabrication processes during synthesis process. Figure 1 shows the block diagram of our BRAINS framework, and the main features of BIST design which generated by BRAINS are shown in below:

1. Provides at-speed testing.
2. Programmable for various March algorithms.
3. Provides diagnosis function.
4. Single port / multi-port memory support.
5. Support SRAM / 1T SRAM / DRAM / register file / flash memory types.
6. Test scheduling function for test time reduction.
7. Resource shared among multiple memory cores for area reduction.
8. Using the Memory Modeling Techniques. it is easy for BRAINS to support modern and customized memory architectures.

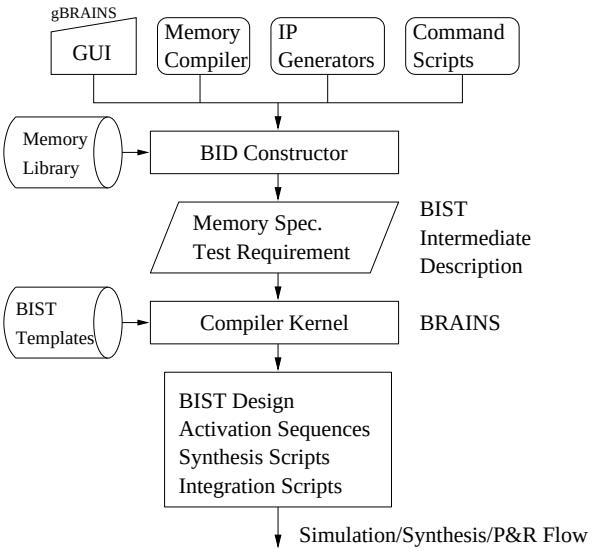

Figure 1: The BRAINS framework