AnaSyC: Static and Dynamic Analysis of SystemC Designs

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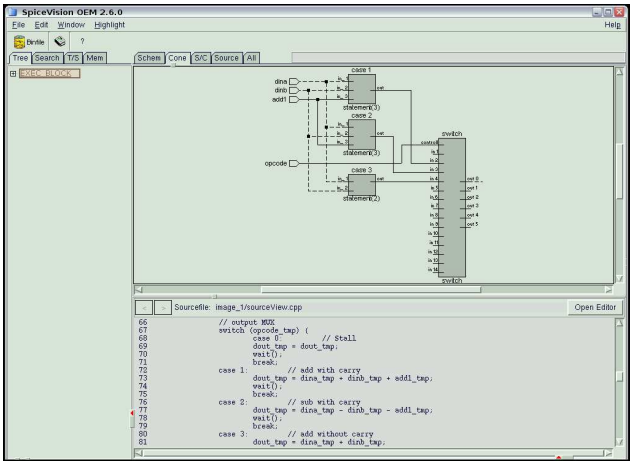
SystemC has become an essential methodology for System Level design, HW/SW Co-Design and early system elaboration. As a result of the broad spectrum of functionality SystemC offers, its models grow in size and complexity. Hence, these models are hard to elaborate manually. To tackle this problem designers append stimuli generators to their SystemC specifications.

We present an approach for analysis of SystemC designs in a dynamic and in a static environment. Our approach has been implemented in the tool *AnaSyC*. The dynamic analysis facilitates designers to investigate circuit properties by offering full control over the run-time progress. An interactive single step simulation enables variable and signal values of the system description to be evaluated. The static analysis consists of a control flow graph (CFG) traversal technique, to discover critical paths and their respective source code. An additional feature of the static analysis is the calculation of cost factors for selected paths of the CFG. The functionality can be broken down to:

- **Single step simulation:** This feature simulates the system model with an executable SystemC specification. Each state-transition of the model can be triggered sequentially.
- **Evaluation of state variables:** In each state the current values of variables and signals can be displayed. The information is taken from the SystemC kernel.
- **Discovery of critical paths:** CFG paths that are frequently used and that are time critical can be indicated for hardware implementation.
- **Cost factor calculation:** Calculates cost factors for a CFG, that is to be selected by the user. This feature enables the direct comparison of different implementations.



The analysis tool *AnaSyC* is part of the SyCE environment [1]. Further details of the previous work can be found in [4, 2, 3].

References

[1] R. Drechsler, G. Fey, C. Genz, and D. Große. SyCE: An integrated environment for system design in SystemC. In *IEEE International Workshop on Rapid System Prototyping*, pages 258–260, 2005.

[2] G. Fey, D. Große, T. Cassens, C. Genz, T. Warode, and R. Drechsler. ParSyC: An efficient SystemC parser. In *Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI)*, pages 148–154, 2004.

[3] C. Genz and R. Drechsler. System exploration of SystemC designs. In *IEEE Computer Society Annual Symposium on VLSI*, Mar. 2006.

[4] D. Große, R. Drechsler, L. Linhard, and G. Angst. Efficient automatic visualization of SystemC designs. In *Forum on Specification and Design Languages*, pages 646–657, 2003.