ARTS – A System-level MPSoC Simulation Framework

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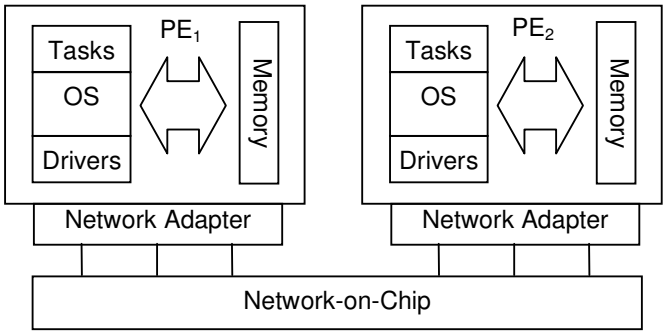
Abstract – One of the challenges of designing a heterogeneous multiprocessor SoC is to find the right partitioning of the application onto the platform architecture. The right partitioning is dependent on the characteristics of the processors and the network connecting them, as well as the application. We present an abstract system-level modelling framework (ARTS) which allows for cross-layer modelling and analysis, covering application layer, middleware layer, and hardware layer. ARTS allow the designer to explore and analyse; the network performance under different traffic and load conditions, consequences of different mappings of tasks to processors (software or hardware) including memory and power usage, and effects of RTOS selection, including scheduling, synchronization and resource allocation policies. In the demonstration we will focus on the programmer's view illustrated through a design space exploration of a multi-mode multimedia application mapped onto an MPSoC platform.

Description: The concurrent and distributed nature of MPSoC systems, means all the layers i.e. application, middleware and hardware need to be represented, if one has to perform meaningful analysis and optimization of a platform architecture for application-specific needs. In the presence of complex communication infrastructure such as Network-on-Chip (NoC), the interaction between these layers (cross-layer dependencies) may impact not only the performance of an individual IP core, but also across the platform, between the IP cores.



For this demonstration, we present an abstract system-level modelling framework, called ARTS, developed at the Technical University of Denmark (DTU). ARTS supports the MPSoC designers in modelling all the hardware and software layers i.e. application, operating system (OS) and platform architecture; and understanding their causalities. The ARTS framework is not developed with any specific problem in mind, but is a modular and extendable framework which allows the modelling of different system characteristics such as applications data flows, OS scheduling, IP execution speeds, NoC topology and protocol. Furthermore, the use of the standard OCP sockets at the IP and NoC boundary allows an easy and seamless integration of IP models described in alternate abstractions, thus allowing mixed-abstraction simulation within ARTS.

To use ARTS, the designer has to provide the following inputs (or make use of available values from within ARTS): (i) application models, described as task graphs, (ii) processing elements (PE), described in technology files, and (iii) user defined architecture and task mapping, described in ASCII file. The framework then instantiates and simulates the prescribed platform. One such platform is illustrated in the figure. The output is a set of ASCII files profiling the runtime or the final system characteristics, such as memory usage, communication contention, PE utilization, etc. These outputs allow the designer to investigate the merits of the simulated platform.

ARTS is implemented in SystemC and the modelling of an MPSoC platform is based on three basic components: the *synchronizer*, the *allocator* and the *scheduler*. The properties of these components allow modelling of a diverse range of PEs and their communication behaviours via the NoC. The *allocator* controls the ownership of resources, such as the execution engine of the processor, or the routers/links of the NoC. The *scheduler* controls the order in which tasks are executed on the resources, i.e. application tasks mapped to a PE or communication tasks in the NoC. The *synchronization* controls the interdependencies, i.e. precedence constraints between application tasks or priorities of communication tasks. Using ARTS, the designer can investigate problems both in the general and the real-time application domain.

In the demonstration we will show the potential of the ARTS framework through a case study carrying out a design space exploration of multi-mode multimedia applications mapped onto an MPSoC platform. The multimedia applications make use of five application programs containing more than 100 tasks. The design space exploration covers architectures with seven possible IP core types and many NoC configurations. This case studies will provide insight into the advantages and trade-offs of introducing NoC against performance parameters such as memory, power and program completion time, i.e. meeting real-time requirements.