Submission form for Working Silicon Demonstration at the University Booth DATE'2006

Deadline for submission: January 9, 2006 Notification of acceptance: February 10, 2006 Full description of the demonstrator: February 17, 2006 Email for submission : schoeber@edacentrum.de

[X] Yes

I submit a hardware demonstration for the university booth at the DATE'2006 and will provide detailed information. In addition, I will provide hardware, software and other necessary or useful information and equipment for the demonstration. During the DATE, a trained supervisor of the demonstration will give the audience the opportunity to view and discuss the demonstration in the agreed time slot. If accepted, I will prepare all appropriate data **until February 17, 2006**.

1/ Organisation

Name of university: National Tsing Hua University, Hsin-Chu, Taiwan Name of institution: EDA Lab, Department of Computer Science Leader of institution: Professor Youn-Long Steve Lin

2/ Contact Person

Name: Professor Youn-Long Steve Lin Post address: Dept CS, National Tsing Hua Univ., Hsin-Chu, Taiwan 300 Phone: +886-3-573-1072 Fax: +886-3-572-3694 E-mail: ylin@cs.nthu.edu.tw Internet address: <u>http://www.cs.nthu.edu.tw/~ylin</u>

3/ Name of the demonstrated circuit:

A Hardwired H.264/AVC Main Profile Video Decoder Prototype

4/ Abstract of the functionality of the circuit and its application environment (not more than 300 characters):

We will demonstrate an H.264/AVC main profile video decoder developed by our laboratory in National Tsing Hua University, Taiwan. Coded in synthesizable Verilog RTL and strictly following guidelines for IP reuse, our design is very small at 170K-gate and power efficient due to innovative algorithm and architecture design. It is integrated in a locally-developed AMBA-based multimedia SOC platform, which has successfully demonstrated JPEG and MPEG4 codec in our previous projects. Running at 30MHz, our FPGA prototype is capable of real-time decoding H.264/AVC main profile CIF video at 30fps.

Professor Lin will talk about this decoder in 2006 DATE Full-Day Tutorial (Tutorial F: Four New Ways to Design a High Definition Video CODEC). It will be especially beneficial to those tutorial attendees if they can see the demo after the tutorial.

5/ Research project of the demonstrator (if there is one):

Name of the project: Leader: E-mail: Internet address: Project partner: Start of the project: End of the project:

6/ One page description of the circuit and its application environment (ASCII, graphics or separate in PostScript or PDF):

Please see attached at the end of this document.

7/ Necessary hardware and software resources (provided by the presenter):

We will bring our own platform board and a notebook PC.

8/ Comments, additional requirements:

A Hardwired H.264/AVC Main Profile Video Decoder Prototype

We present a hardwired decoder prototype for H.264/AVC main profile video. Our hardware functional blocks include variable-length decoding, CABAC decoding, inverse quantization and inverse DCT, motion compensator, intra compensator, and deblocking filter. They communicate with one another via memory buffers and are integrated and controlled by a main controller. The whole decoder is wrapped with an AMBA-AHB wrapper such that it can be reused as a silicon IP. The following two figures depict the block diagram and SOC platform, respectively, of our system.

