Turbo Tester: A CAD Software for Digital Test

Turbo Tester (TT) is a test software package developed at the Department of Computer Engineering of Tallinn University of Technology. The TT software consists of the following test tools: test generation by different algorithms (deterministic, random and genetic), test set optimization, fault simulation for combinational and sequential circuits, testability analysis and fault diagnosis. It includes test generators, logic and fault simulators, a test optimizer, a module for hazard analysis, BIST architecture simulators, design verification and design error diagnosis tools (see Fig. 1). TT can read the schematic entries of various contemporary VLSI CAD tools that makes it independent of the existing design environment. Turbo Tester versions are available for MS Windows, Linux, and Solaris operating systems.

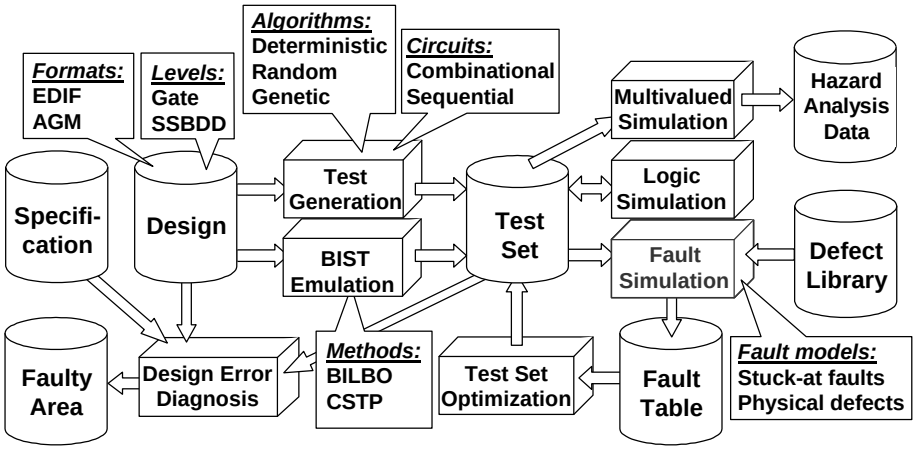

Fig.1. Turbo Tester environment

The main advantage of TT is that different methods and algorithms for various test problems have been implemented and can be investigated separately of each other or working together in different work flows.

Model Synthesis. All the tools of TT use Structurally Synthesized BDD (SSBDD) models as an internal model representation. TT includes a design interface generating SSBDD-s in AGM format from EDIF netlists. The set of supported technology libraries can be easily extended.

Test Generation. For automatic test pattern generation (ATPG), random, deterministic and genetic test pattern generators (TPG) have been implemented. Mixed TPG strategies based on different methods can also be investigated. Tests can be generated both for combinational and sequential circuits.

Test Pattern Analysis. There are concurrent and parallel fault simulation methods implemented in the system.

Test Set Optimization. The tool is based on static compaction approach, i.e. it minimizes the number of test patterns in the test set without compromising the fault coverage.

Multivalued Simulation. In Turbo Tester, multi-valued simulation is applied to model possible hazards that can occur in logic circuits. The dynamic behavior of a logic network during one single transition period can be described by a representative waveform on the output or simply by a corresponding logic value.

Design Error Diagnosis. After a digital system has been designed according to its specification, it might go through a refinement process in order to be consistent with certain design requirements, e.g., timing specifications. The changes introduced by this step may lead to undesired functional inconsistencies compared to the original design. Such design errors should be identified via verification.

Evaluation of Built-In Self-Test (BIST) Quality. The BIST approach is represented by applications for simulating logic BIST and Circular Self-Test Path (CSTP) architectures.