SyCE: An Integrated Environment for System Design in SystemC

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Abstract We present a system design environment for SystemC (www.systemc.org) called SyCE. It consists of several components for efficient analysis, verification and debugging of SystemC designs. The core tools are:

- ParSyC [1]: A parser for SystemC designs that has also some synthesis options, i.e. netlists can be generated.
- CheckSyC [2]: A formal verification tool for equivalence checking and property checking.
- DeSyC [3]: A tool for automatic debugging and error location in netlists.
- ViSyC [4]: A visualization tool for schematic and source code view supporting cross-probing and annotation of simulation and debugging results. ViSyC makes use of the visualization engines from Concept Engineering (www.concept.de). A screenshot is shown in Figure 1.

The tools fully support hierarchy and are tightly interacting. Designs can be described at different levels of abstraction. The overall flow is shown in Figure 2.

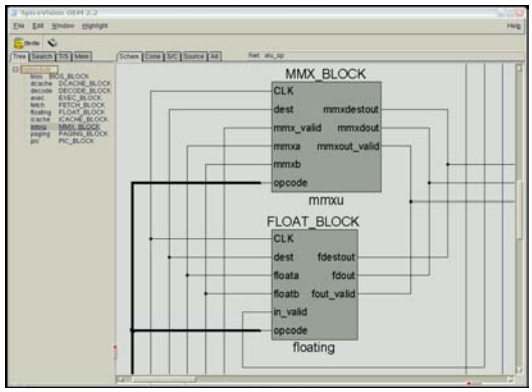

Figure 1: Screenshot of ViSyC

References

[1] G. Fey et al, ParSyC: An Efficient SystemC Parser, SASIMI, pp. 148-154, 2004
[2] D. Große, R. Drechsler, CheckSyC: An Efficient Property Checker for RTL SystemC Designs, ISCAS, 2005
[3] G. Fey, R. Drechsler, Efficient Hierarchical Debugging for Property Checking, Tech.Rep., 2005
[4] D. Große, et al. Efficient Automatic Visualization of SystemC Designs, FDL, 2003

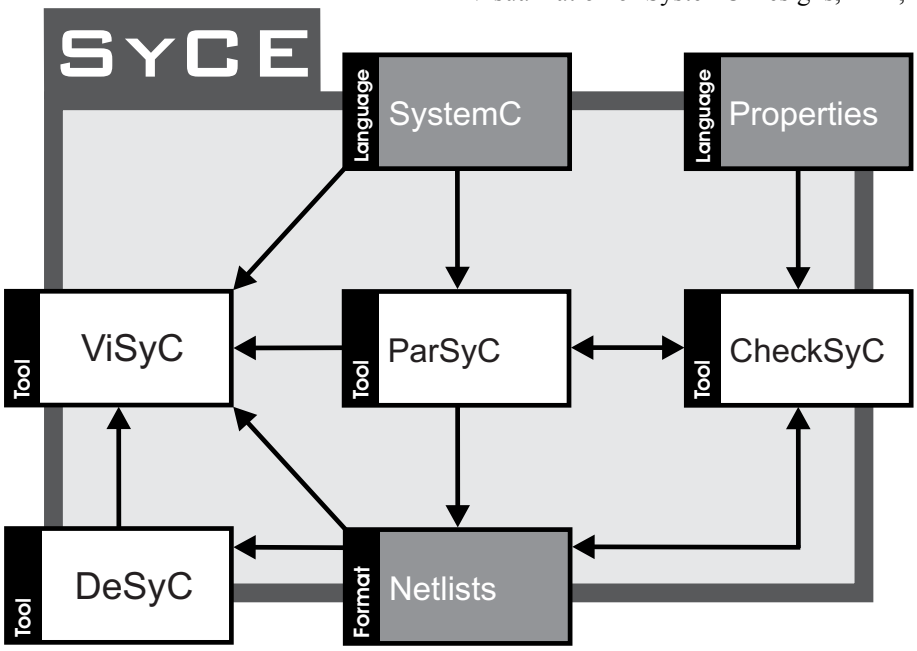

***Figure 2*:** Overall flow of SyCE