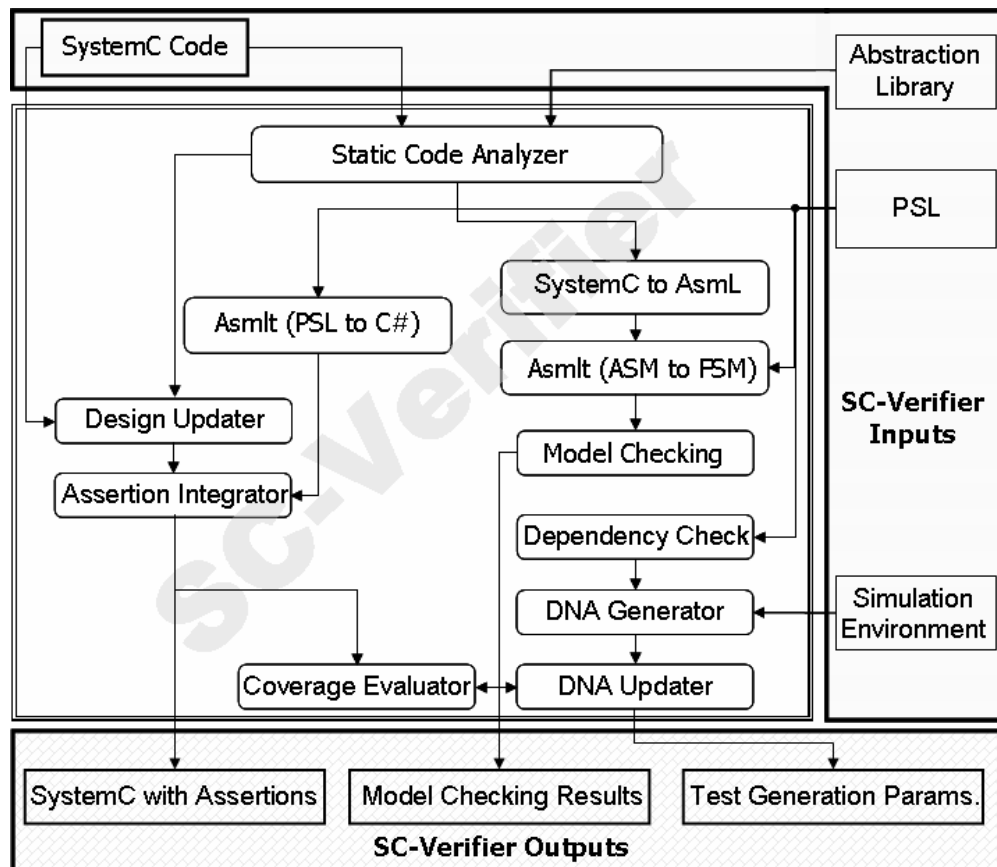# SC-Verifier: A Tool for SystemC System Level Verification

SC-Verifier is a tool for the verification of system level designs modeled in SystemC. It includes a static analysis module to abstract SystemC designs; hence, reducing their complexity for better model checking and assertion based verification results. The static analysis is based on abstract interpretation techniques, which can handle large and complex designs. For model checking, the reduced model is first translated to AsmL (Abstract State Machines Language), a language enabling a higher level of abstraction and an interface for multiple model checking and theorem proving tools such as SMV and PVS. We also provide the model checking of design properties written in PSL (the property specification language standard) by adapting a reachability algorithm embedded in the Asmlt tool from Microsoft. We embedded the PSL language in AsmL, where the user defines directly the design properties in AsmL according to the PSL syntax. When the model checking does not terminate due to state explosion, we complete the verification process by enabling assertion based verification. For instance, the PSL assertions are compiled to generate a set of C# modules that are plugged in read-only mode to the SystemC design then verified by simulation. Furthermore, we embedded a genetic algorithm to guide the test vectors generation in order to enhance the simulation coverage. Our tool has shown promoting results when applied to commercial standard designs such as the PCI and AGP buses and the look-aside interface[1]. Its performance has been compared to other commercial tools such as RuleBase from IBM and FormalCheck from Cadence.

---

[1] More details are available at: http://hvg.ece.concordia.ca/.