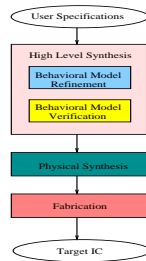


RAMS: A VHDL-AMS Code Refactoring Tool Supporting High Level Analog Synthesis

Kaiping Zeng, Sorin A. Huss

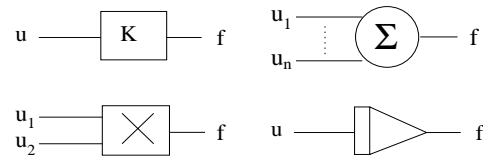
Goals

- High Level Analog Synthesis
- Behavioral Model in VHDL-AMS
- Code Refactoring Methodology
 - Comprehensibility
 - Expandability
 - Reusability
 - Synthesizability



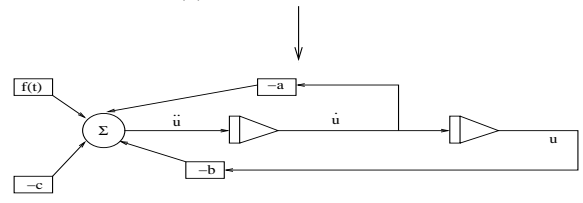
Partition of DAE

- Analog Functional Primitives

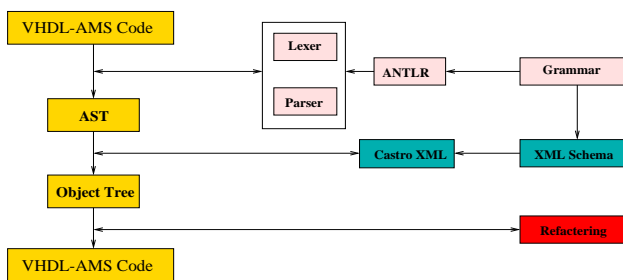


- Mapping of DAE to Primitives

$$f(t) = \ddot{u} + a\dot{u} + bu + c$$



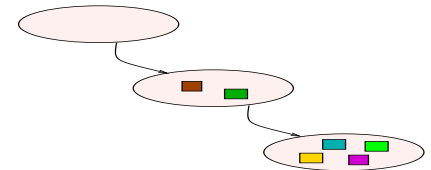
Automated Procedure



- Grammar of VHDL-AMS
- Parser Created by ANTLR
- Object Tree Generated with Castor XML
- Code Refactoring Algorithms

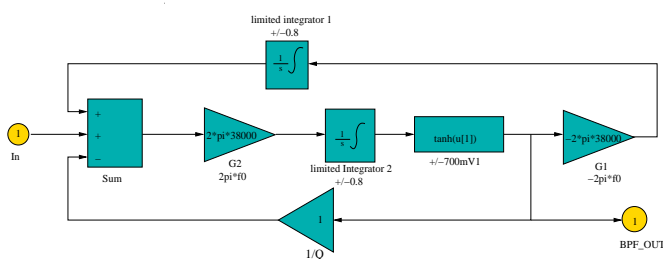
Code Refactoring

- Dataflow-oriented
- Controlflow-oriented
- Structure-oriented
- Dislocating
- Concretizing

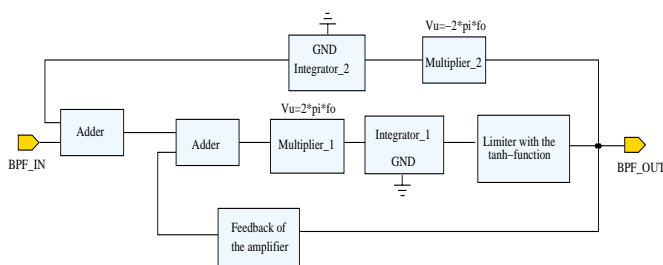


Signal Flow Model vs. Conservative Model

- Signal Flow Model: Pure mathematical description of input/output behavior

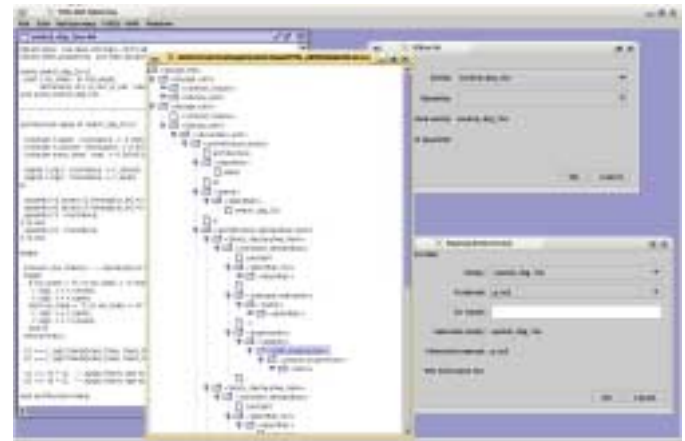


- Conservative Mode: Conservation laws have to be satisfied on pins



Tool Implementation

- Developed with Eclipse
- Java as Implementation Language



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