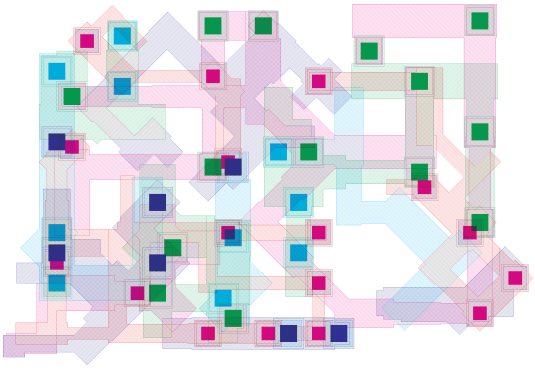
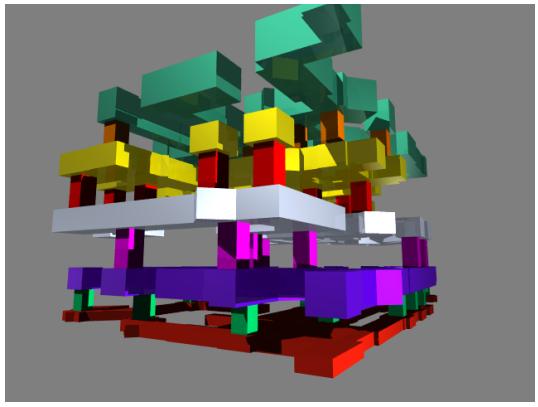
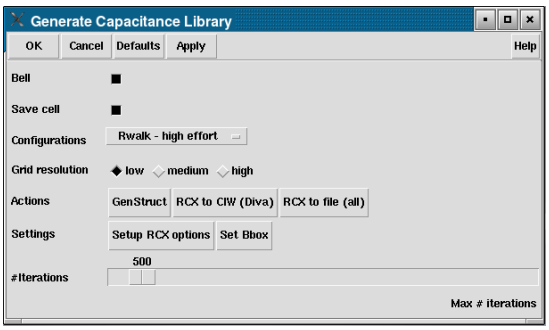
Automated Generation of Metal Interconnect Structures for Benchmarking Parasitic Extraction Tools.



To perform a comparative parasitic extraction tool analysis, it is desirable to use not only a few extraction tools, but as many as possible and from different EDA companies. Moreover, various topologies and interconnect structures have to be extracted to create a data base large enough for statistical analysis.
These requirements call for a completely automated tool flow comprising random generation of complex interconnect layouts (see on the left and below), parasitic extraction with each tool and data storage. Without such an automated tool flow, human interaction would significantly slow down the whole data generation process due to the high number of design steps which usually must be performed by engineers.



To achieve this task, a software solution is presented, which uses various software components from the Cadence IC framework, such as the Virtuoso layout tool and the built-in script language SKILL. Furthermore, parasitic extraction tools from Cadence, Mentor Graphics and other companies are used for comparison. Since such an automated tool linkage and data exchange interferes with low-level tool functions, extensive use of the software support platform Sourcelink from Cadence was made, which was only accessible through the SEED cooperation.
The automatic layout generation program consists of a set of Skill routines for Cadence Virtuoso, which we were developed. The underlying algorithm represents a random-walk based trial-and-error approach which employs on-the-fly DRC-checking. It randomly generates complex interconnect structures which are then used for the parasitic extraction process. The related user dialog is shown above, it is used to specify various parameters for the random-walk algorithm, such as step size, area and effort and to determine the number of iterations (i.e. structures being generated).



After the generation of the data base, the different parasitic values, (e.g. capacitance) can be compared and analyzed. On the right, the distribution of the capacitance from Diva and Assura (no field solver option used) with respect to the capacitance from Assura with field solver option is shown.