The Erlangen Slot Machine (ESM): A flexible Platform for Dynamic Reconfigurable Computing

Christophe Bobda, Mateusz Majer, Ali Ahmadinia, Thomas Haller, André Linarth and Jürgen Teich

Departement of Computer Science 12
University of Erlangen-Nuremberg
Am Weichselgarten 3, D-91058 Erlangen

email: {bobda, majer, teich}@cs.fau.de

Introduction

Xilinx FPGAs, one of the few partially reconfigurable devices offer enough logic to efficiently implement resource demanding applications which arise in video, audio and signal processing as well as in other fields like mechanical control. Partial reconfiguration is useful to increase the flexibility in computation and time-sharing of device space. However this feature cannot be use on the most available systems.

Many systems on the market offer various interface for audio and video capturing and rendering, for communication and so forth. However, each interface is connected to the FPGA using dedicated pins in a fixed location. Modules willing to access a given interface like the VGA must be placed in the area of the chip where the FPGA signals are connected. With this, the development process of modules for todays FPGAs is very tedious and the relocation even more difficult and not automated.

For example a module placed at a given location on the device is implicitly assigned all the resources in that area. This includes the pins, the clock managers and other hard macros like multipliers and BlockRAM. Each module using resources outside its placement area must go through other modules in which area the needed resource are located. This situation has three negative consequences: 1) Module development: Automatizing the development of modules for partial reconfiguration is difficult. 2) Intermodule communication: Placed modules must be able to communicate with other modules independent of their placement position. 3) I/O pin constraints: Modules accessing I/O pins are not relocatable, because each pin has a fixed physical location.

The purpose of the **Erlangen Slot Machine** is to overcome the deficiencies of existing FPGA platforms by providing:

1. Maximal reconfigurability through a flexible architecture allowing unrestricted partial reconfiguration
2. Module development support

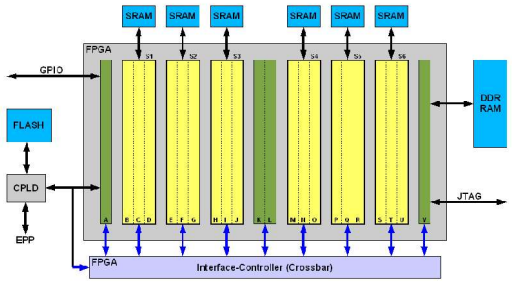
ESM Architecture

With the limitation of existing platforms in mind, we developed a new platform concept called **ESM**. The platform consists of a BabyBoard featuring a Virtex II-6000 FPGA from Xilinx, several SRAM banks and a configuration circuit. The flexibility of partial reconfiguration is maximized here by providing a separable **BabyBoard** which can be mounted on different **MotherBoard** types.

ESM BabyBoard

The main components on the BabyBoard are:

1. The main FPGA: The main FPGA is a Xilinx Virtex II 6000/8000 connected to different interfaces.
2. Configuration circuit which consists of an FPGA Spartan II use to configure the main FPGA and a CPLD used to download the Spartan II configuration on power up.
3. A Flash with 64 Mbyte capacity is available to enable the storage of up to 32 full configurations.



4. Six SRAM banks with 2 MByte each are vertically attached to the board, thus providing enough memory space to six different slots for temporal data storage. The SRAMs can be also used for shared memory communication between neighbor modules, e.g., for streaming applications. The SRAMs are connected to the FPGA in such a way that the reconfiguration of a given module will not affect the access to other modules. The connection to the SRAMs is realized in the north of the device.
5. Interface Access: Interface pins are available in the south of the device. Several modules placed on the device can therefore access their interface device like video and audio input and output, high speed communication, etc. using the south ports. The connection to the interfaces is dynamically switched through a run-time programmable FPGA on the MotherBoard realizing the interface controller.

ESM MotherBoard

Actually, we provide only one type of MotherBoard that is mainly targeted to develop applications in multimedia and signal processing. The MotherBoard provides programmable links to all peripherals.

Their links are established through a programmable crossbar implemented in a dedicated FPGA. This crossbar functionality basically solves the I/O pin dilemma of all existing FPGA platforms, thus allowing free relocation of modules requiring I/O pin connectivity. Free module relocation is possible via a configuration manager on the BabyBoard.

ESM Communication among placed modules

The communication among different modules placed in the slots of the BabyBoard can be done in three different ways: The first one is a direct communication using Bus-Macros between the modules. The second one is the shared memory using the SRAMs or the BlockRAMs. However, those two communication modes can be used only by neighboring modules. For modules placed in non-adjacent slots we provide a dynamic signal switching communication architecture called reconfigurable multiple bus (RMB) which allows two modules willing to communicate at run-time to set up a communication link in order to exchange data. The communication link is destroyed at the end of the communication, thus providing free channels for new communications.