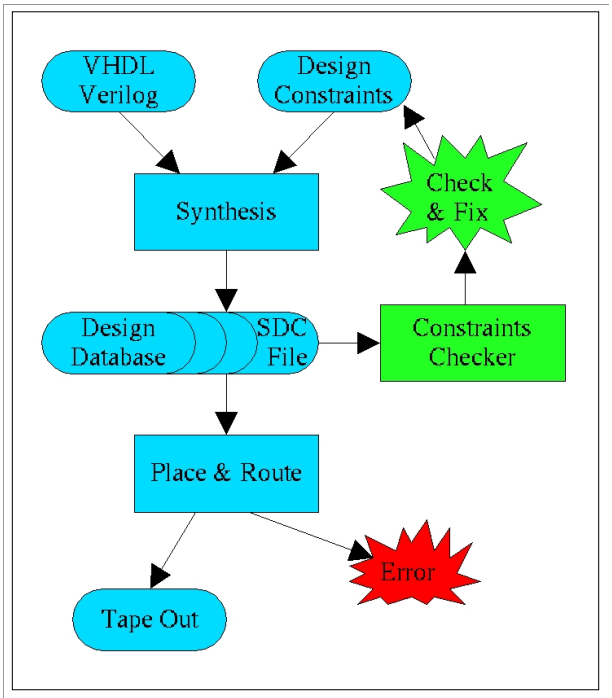
SIEMENS

ElectronicDesignHouse

Chip Design Constraints Checker

In today's digital Integrated Circuit design environments, the tools used for Front End Design and Back End Layout are typically from different vendors. Due to the incompatibility, layouters often experience problems, because their tool can not deal with the constraints created by the synthesis tool. This leads to errors, several days later, during the layout. A complete redesign is then necessary.



Based on this practical experience, the Chip Design Constraints Checker has been developed by Siemens Electronic Design House for Infineon Technologies.

The Chip Design Constraints Checker performs several checks in the early stage of a design and uncovers errors which would not normally appear until placement or routing. The design engineer can fix those errors before transferring a design to the layout tool.

The Chip Design Constraints Checker can easily be adapted to almost every design flow running on Workstation or PC. Tools from the following CAD vendors are supported: Synopsys, Avant!, Magma and Cadence. Other vendors on request.

For further information contact:
Peter Kaiser
Tel.: +49 (0)89 636 47889
Email: peter.kaiser@mchr2.siemens.de
Web: http://www.eda−services.de